
TOMORROW starts here.
cisco
Cisco live!

# Cisco Enterprise Silicon – Delivering Innovation with UADP and QFP

BRKRST-3640

Dave Zacks

Distinguished Systems Engineer

Cisco live!

# Cisco Enterprise Silicon –
## Delivering Innovation with UADP and QFP

### BRKRST-3640 – **Session Overview and Objectives**

**Come to this session to learn about the latest advances in Cisco Enterprise silicon development –** ASIC (Application Specific Integrated Circuit) hardware which provides a key foundational element of the Cisco ONE Architecture for Enterprise Networks, and which support key industry trends such as SDN.

**Attendees at this session will gain a greater insight into how ASICs are created, showcasing the advanced capabilities and functionality delivered by two of Cisco's latest switching and routing silicon innovations UADP (Unified Access Data Plane) and QFP (QuantumFlow Processor).** By developing custom silicon, and leveraging this advanced hardware within our Enterprise portfolio, Cisco has always provided differentiating capabilities and compelling customer value across many platforms.

In this session, we will **explore the capabilities and advantages** provided by custom Cisco silicon, **provide greater insight** into the functionality delivered by existing Cisco Enterprise ASICs, and **explore the new capabilities and solutions** enabled by Cisco's latest generation of Enterprise-focused programmable switching and routing chipsets UADP and QFP.

# Cisco Enterprise Silicon –
## Delivering Innovation with UADP and QFP

## Your Instructor Today … **Dave Zacks**

I am a **Distinguished Systems Engineer**, and have been with Cisco for 14+ years.

I work primarily with large, high-performance Enterprise network architectures, designs, and systems. I have over 20 years of experience with designing, implementing, and supporting highly available network systems and solutions that have included many diverse network technologies and capabilities, using multiple different topologies.

I have a strong interest in ASIC hardware and solutions – a passion I hope to share with you via this presentation! ☺

**Dave Zacks**
Distinguished Systems Engineer
dzacks@cisco.com

# AGENDA

Why ASICs?
How is an ASIC developed?
Merchant vs. Custom
Cisco ASIC History
The Move to Programmability
QFP
UADP
Summary

# AGENDA

Why ASICs?

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UADP

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# What is an ASIC?

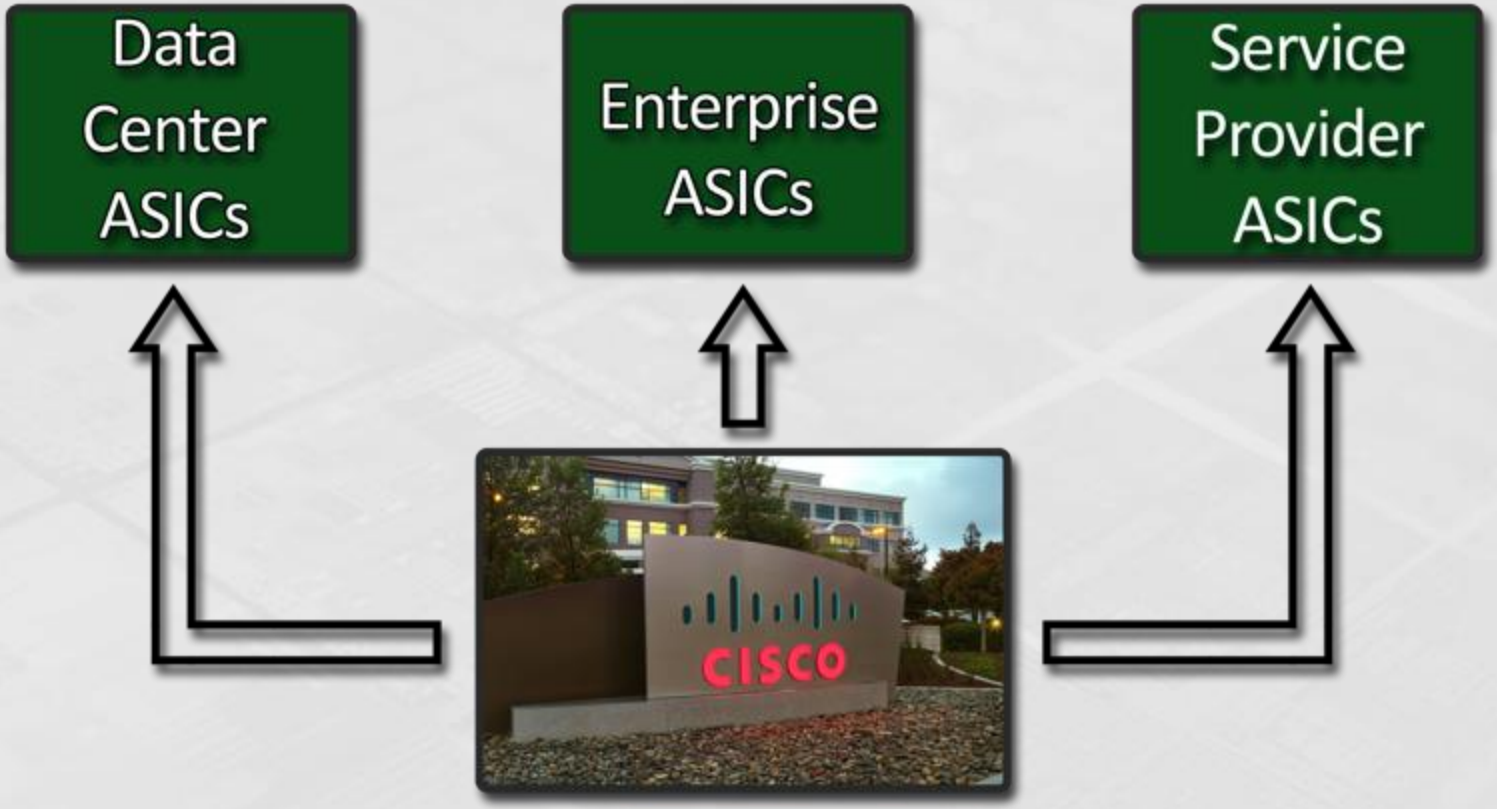
"An *Application Specific Integrated Circuit* is an integrated circuit customised for a particular use, rather than intended for general purpose use…"

# Why Talk ASICs?

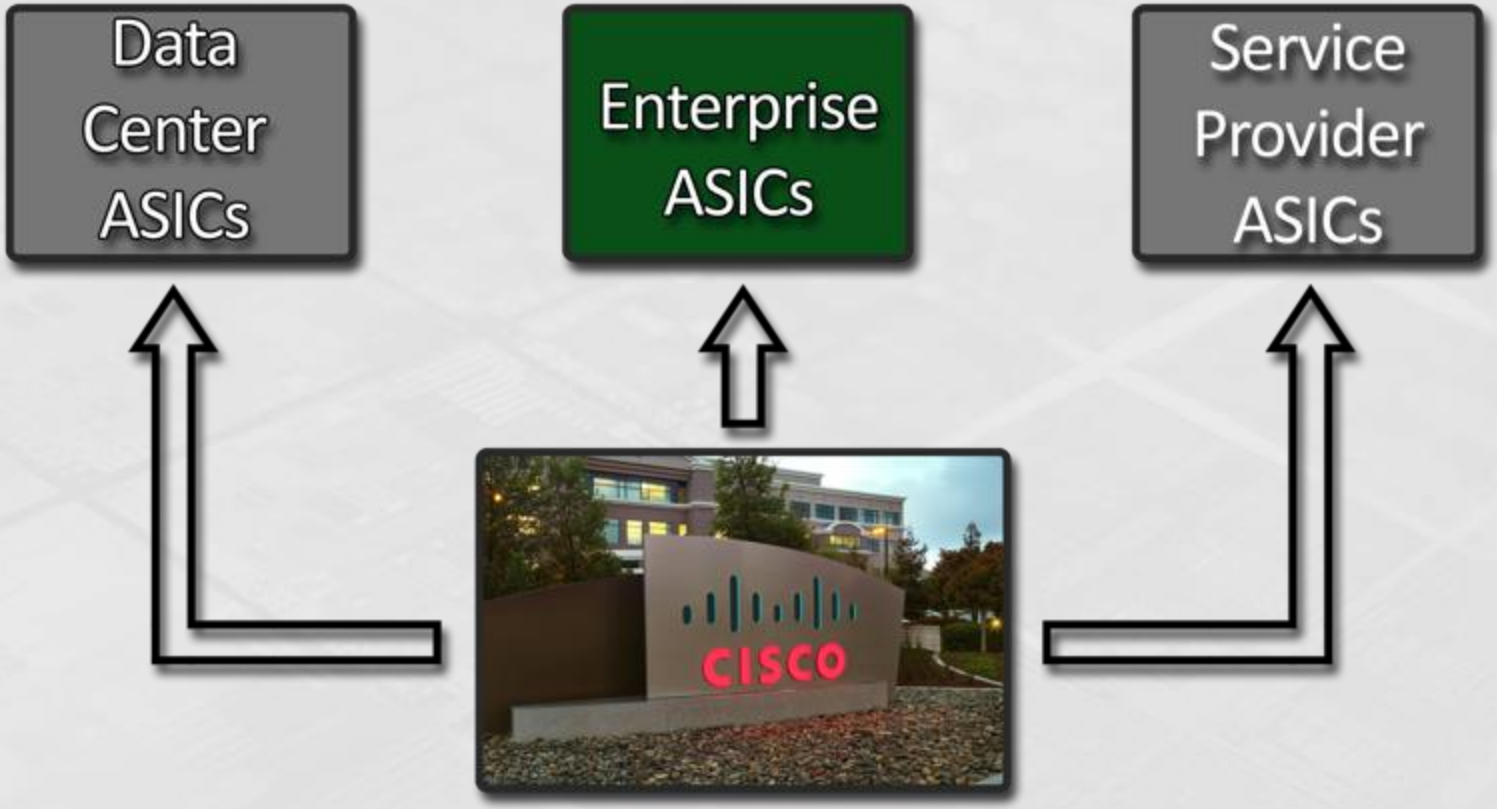

**Rob Lloyd**

Cisco President

Cisco Live Orlando




Cisco has a wide portfolio of ASICs




This presentation focuses on Enterprise only


# ENG Architectural Template

Network Application Layer

Control Layer

Network Element Layer


# Where ASICs Play…

Network Application Layer

Control Layer

Network Element Layer

# AGENDA

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# How is an ASIC built?

R&D

Competition

Market Transitions

Customers

Investment Protection

Tech Trends

Marketing

ASIC Micro Architecture Document

Engineering

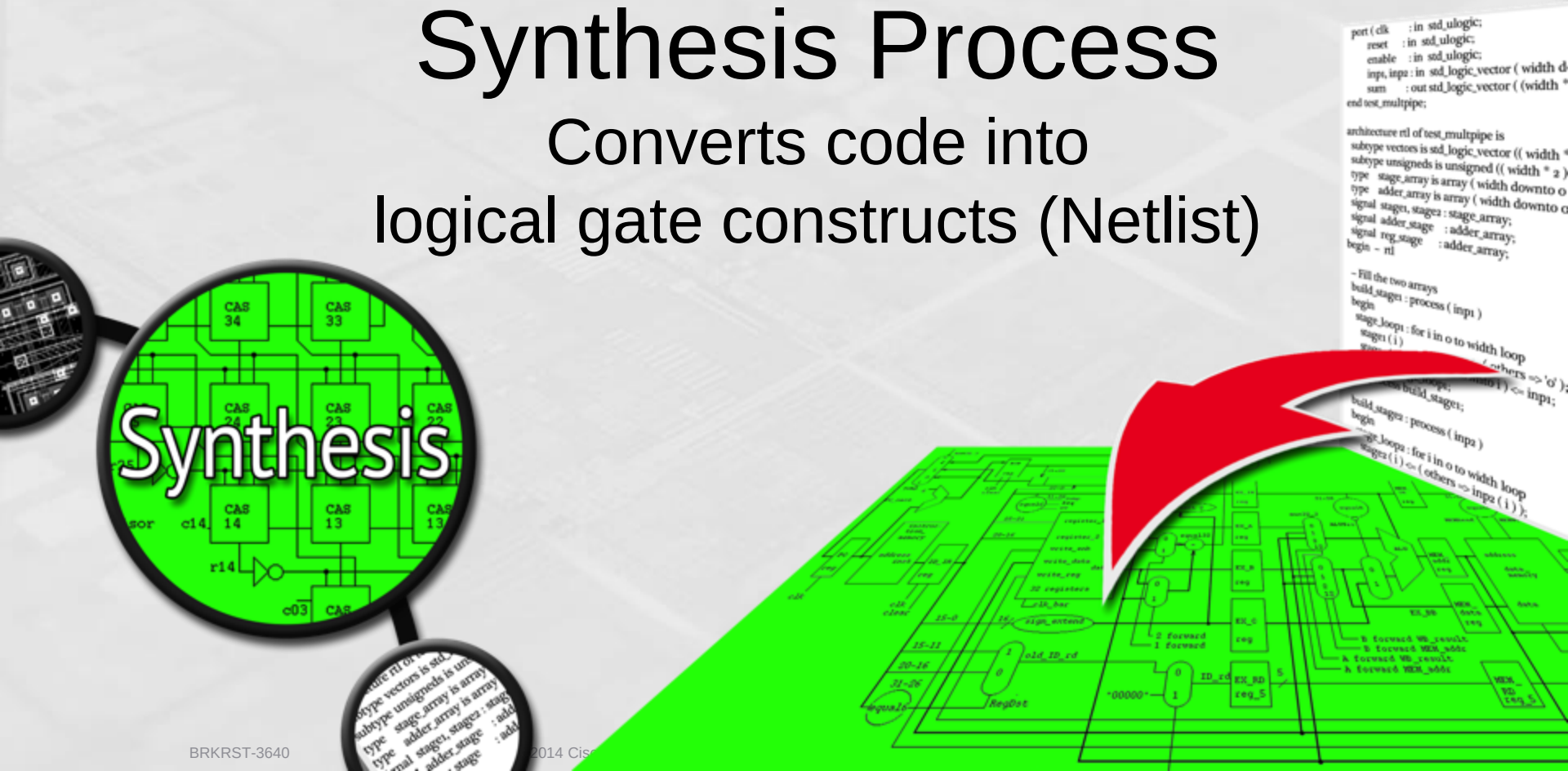
# Then, it starts with coding…


Verilog
VHDL

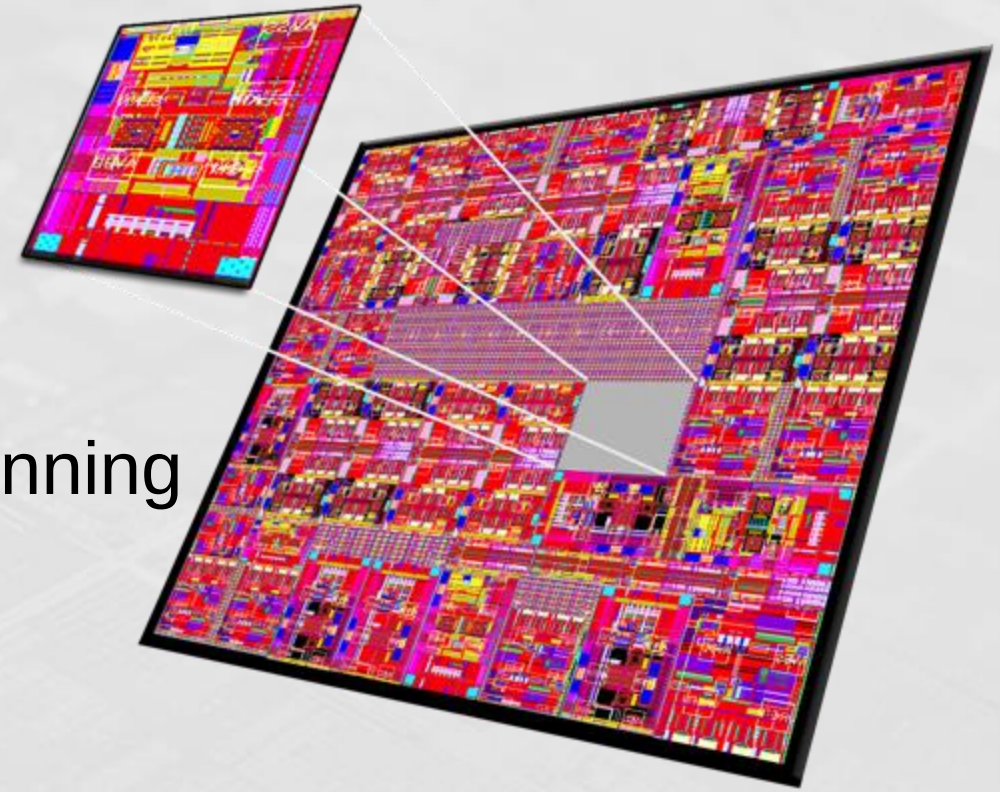
RTL – Register Transfer Level

# Synthesis Process

## Converts code into logical gate constructs (Netlist)



# Floor Planning & Placement



Floor planning


Arrange and interconnect constructs, connect power, minimize crosstalk, etc…

# Imprint design on Silicon Wafer

# Validation of Chip functionality

# Some manufacturing considerations…

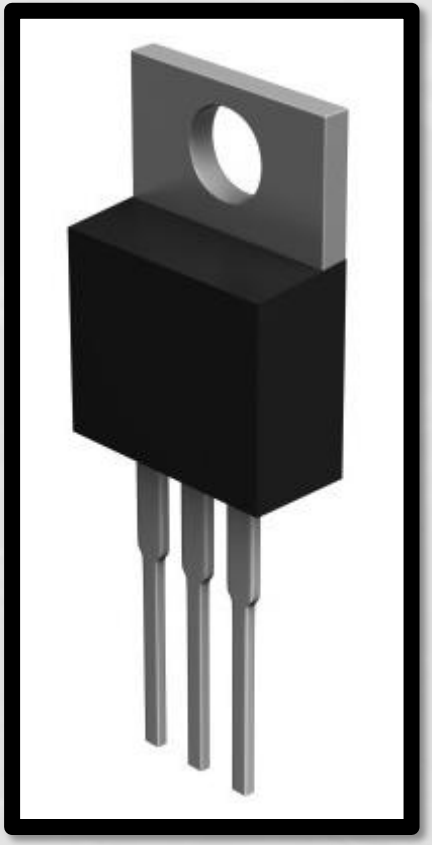
# Sometimes we question if size matters??

In the ASIC world

the smaller the better!

# We are talking transistors…

and how many we can pack in an ASIC die …

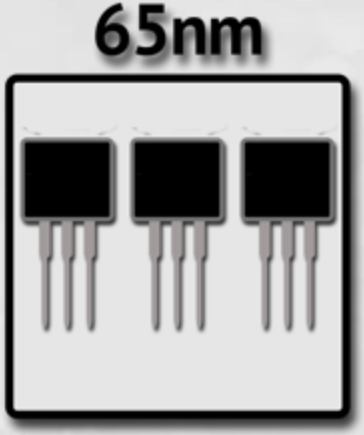


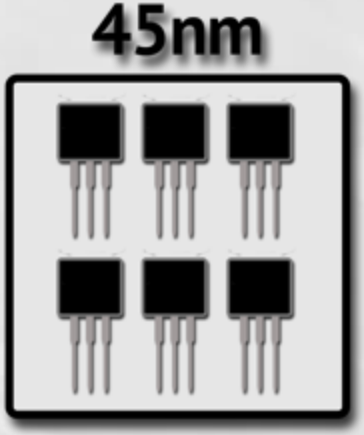
Gordon Moore

"The number of transistors incorporated into a chip will approximately double every 24 months …"

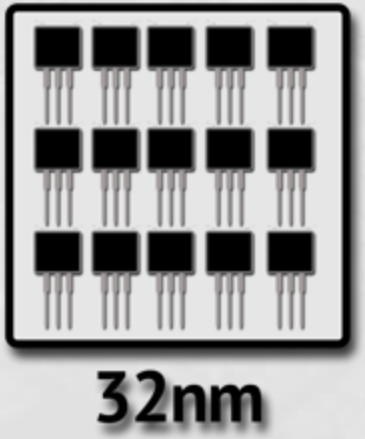
"Moore's Law" - 1975

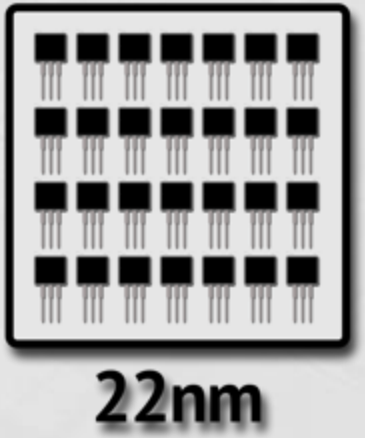
# Transistor Width measured in Nanometers

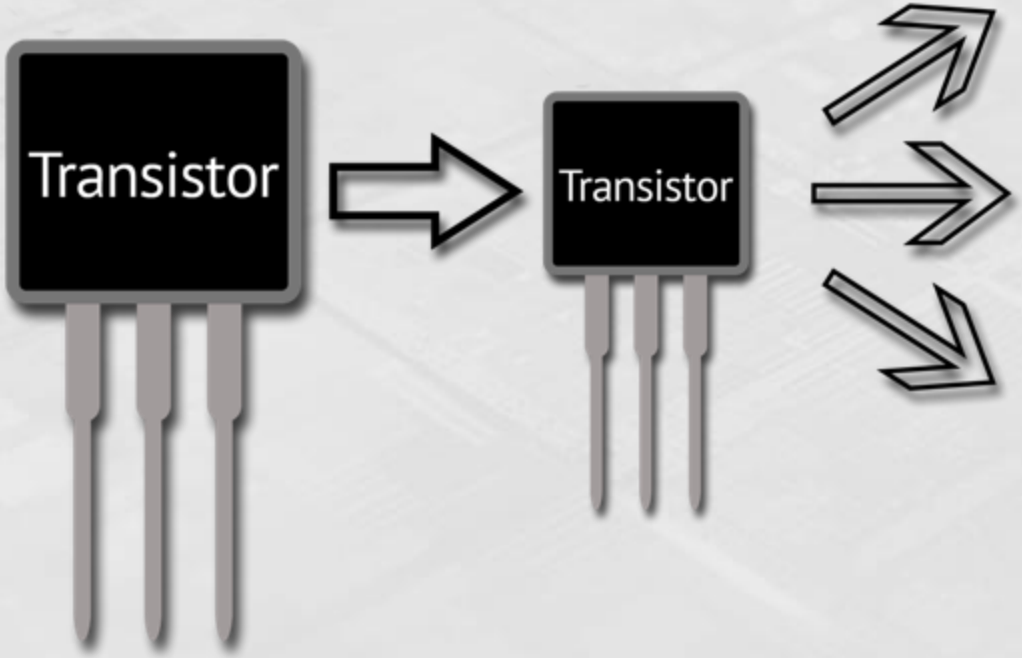




Nanometer = One Billionth of a Meter



# Use of smaller technology leads to benefits …




Lower Price

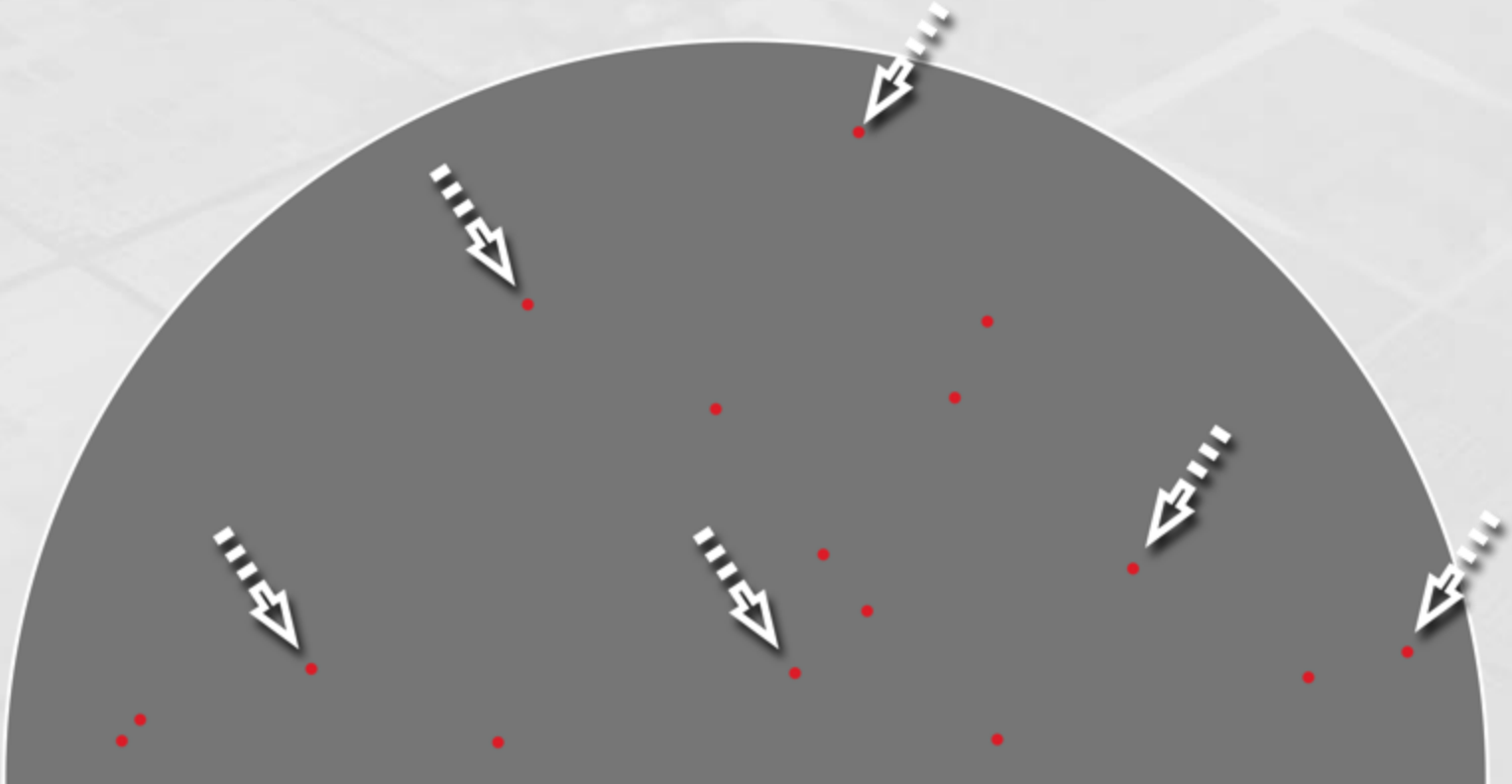
Lower Power


Higher Performance

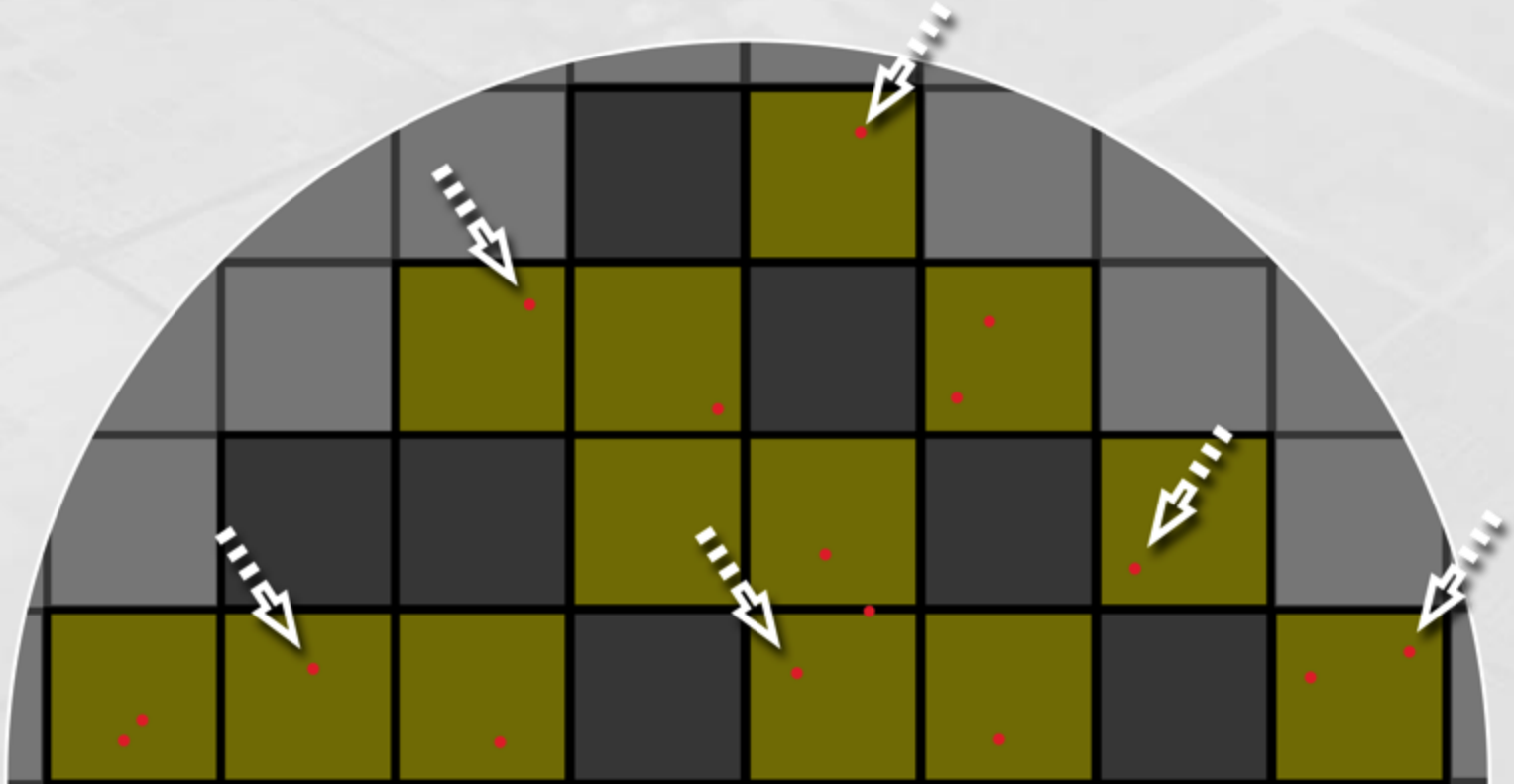
# Let’s explore the question of Yield …

# The Silicon Wafer

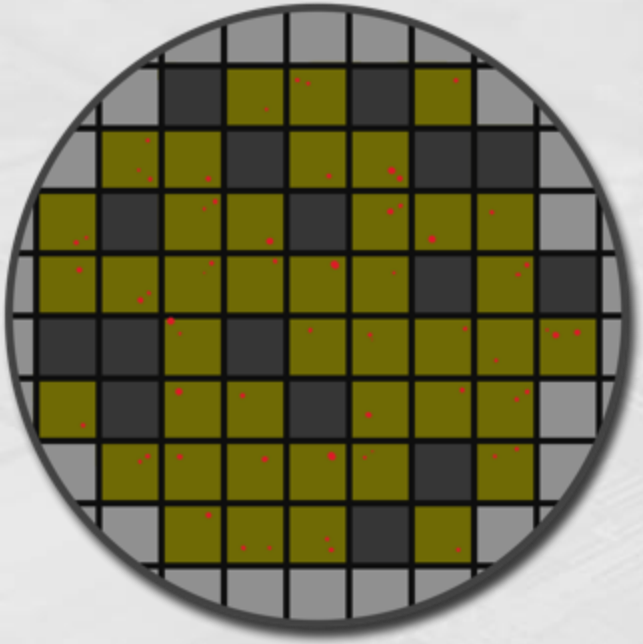
# Every Wafer Has Impurities



# Problem hits after masking …



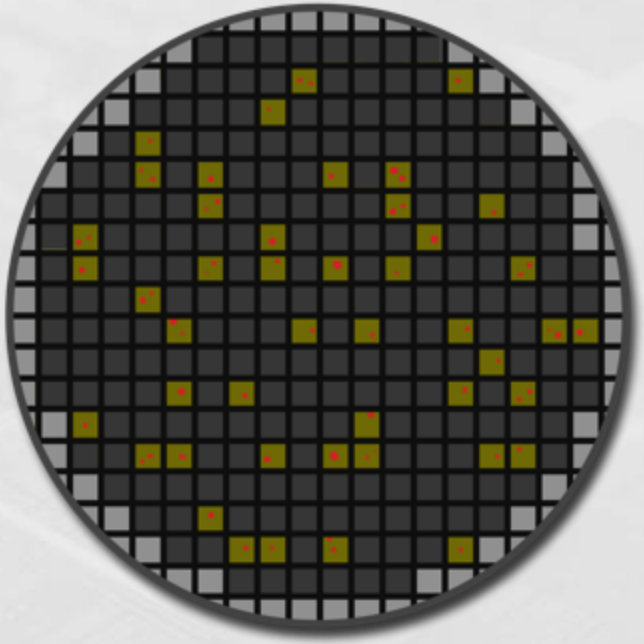
# Not all ASICs are good …



Die Size : 40mm x 40mm

Good: 16 | Bad : 42

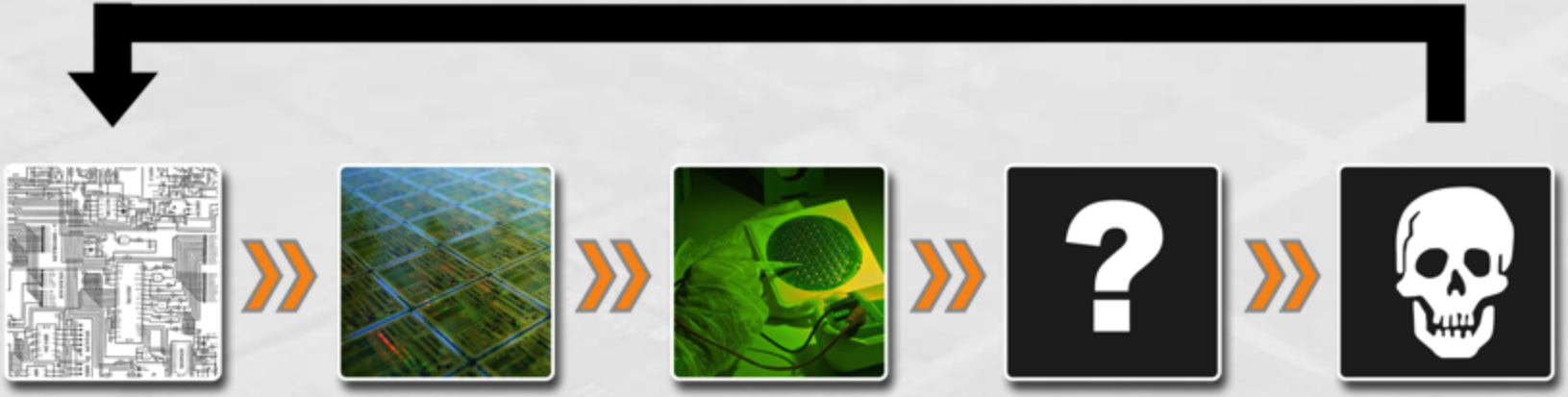
Yield : 27.6%



Die Size : 20mm x 20mm

Good: 212 | Bad: 46

Yield : 82.2%




# ASIC Re-Spin (if needed)

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BROADCOM

MARVELL

intel

Mellanox

# Custom vs Merchant

CISCO

# Why Merchant?


**Time to market opportunities**

Specifications meet customer requirements

Standard based capabilities

# Why does Cisco develop our own silicon?





# Five Reasons Why

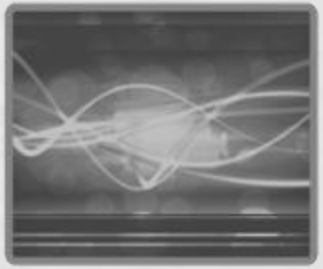




# Innovation

*Examples*

New Functionality (CAPWAP, VxLAN, etc)
Low Latency Switching
Advanced QoS
Security Enhancements
Programmable Pipeline





# Optimisation

*Examples*

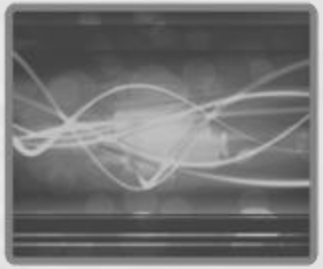
Integrated Stacking Support

Rapid Recirculation (Encapsulations)

Advanced Functionality (VSS, StackPower)

Visibility (Full NetFlow)

Security (MACsec, SGTs)

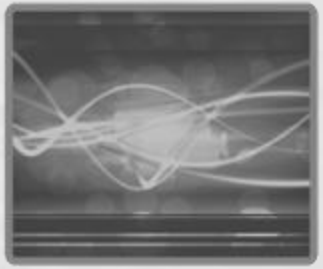




# Economies of Scale

Cisco Total Silicon Business is several times the size of competitors

We deploy our ASICs into some of the largest run rate platforms in the industry





# Leading the Market

*Examples*

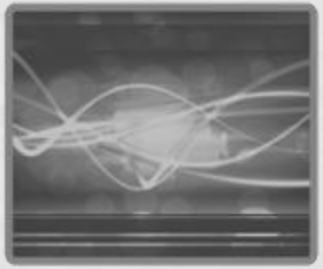
Wired / wireless integration (CAPWAP)

Instant Access (VNtag)

TrustSec (SGTs, SGACLs)

SDN (OpenFlow, ONEpk)

Advanced QoS and Traffic Visibility





Delivering Business Value

Simplified Deployment Options
Better Insight and Optimisation
Increased Security
Most Appropriate Scalability
Flexibility and Investment Protection
*(programmability)*

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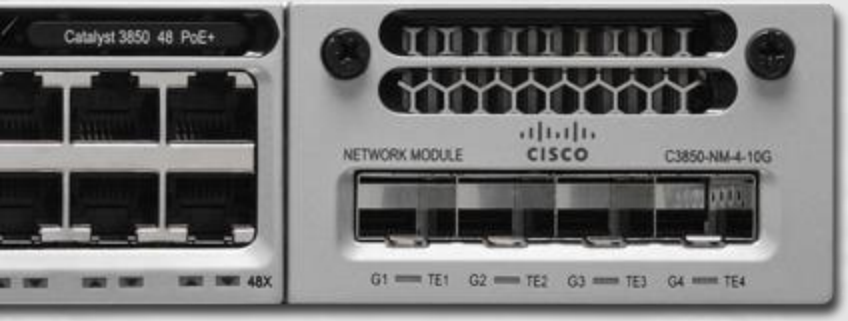
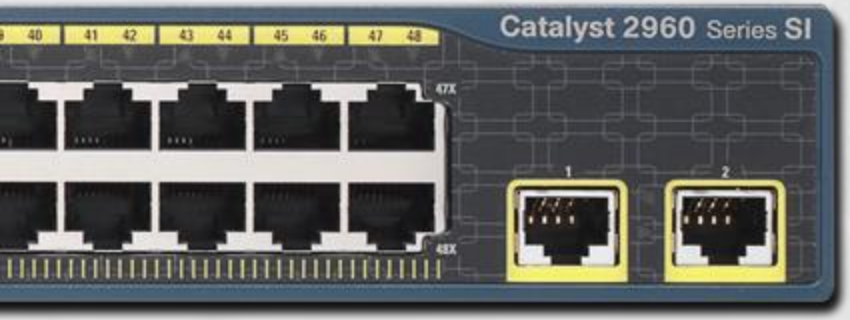
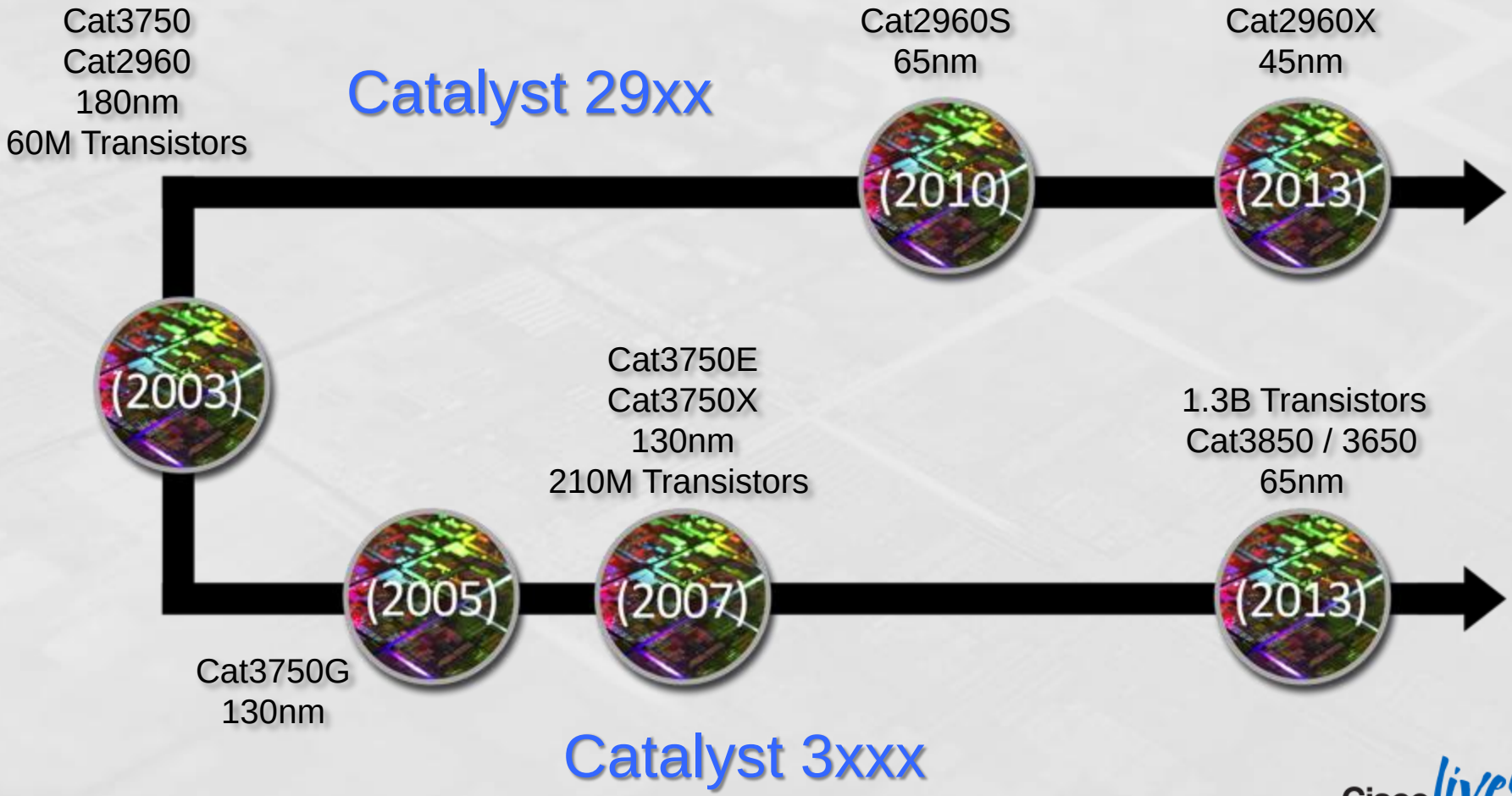
# Cisco has a Long History of Enterprise Switching ASIC Innovation …




# Catalyst 29xx | 37XX | 38XX

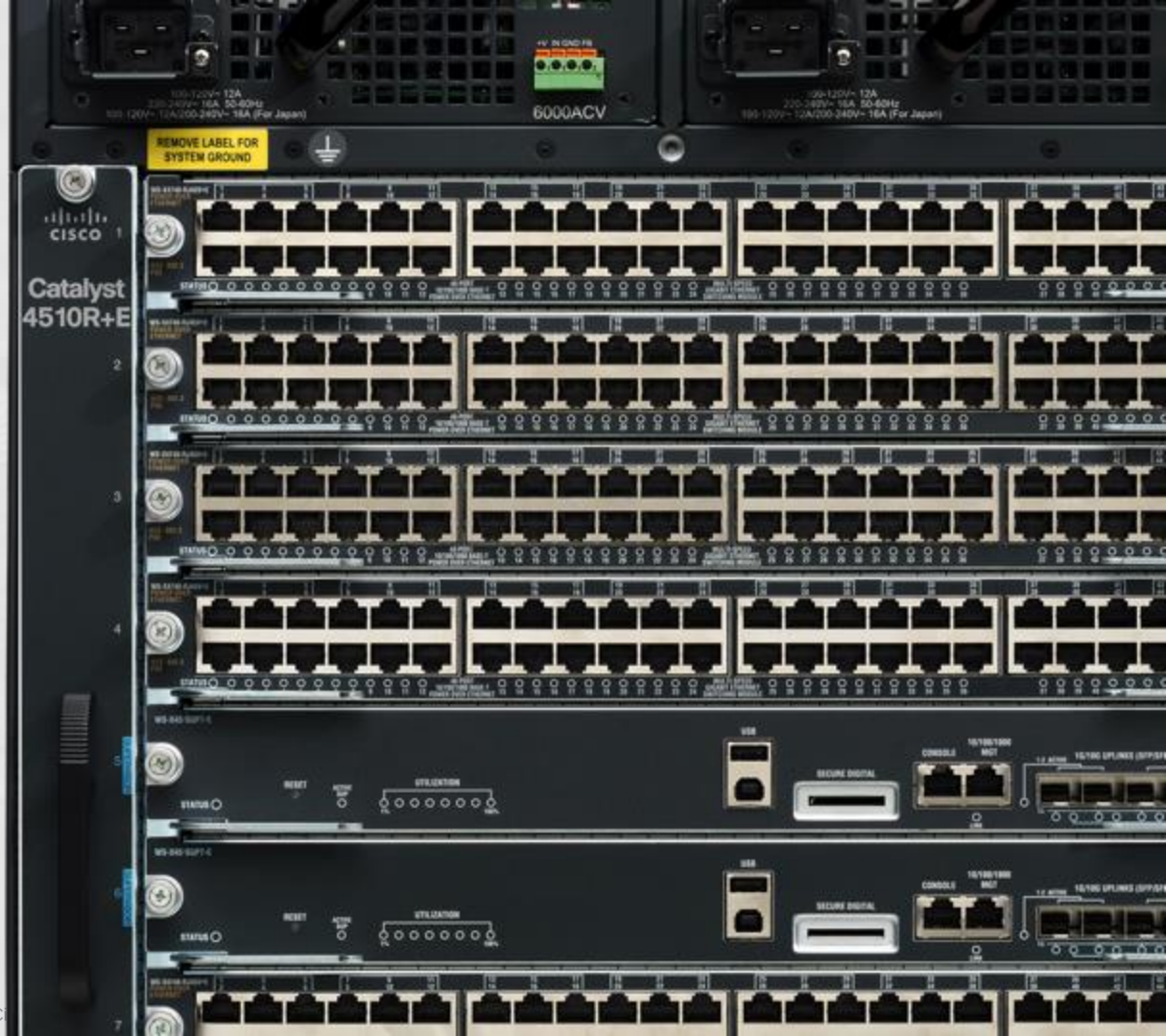




# Catalyst 29XX/3XXX ASIC Innovation

Support for StackWise stacking (32G stack), IPv4 Unicast and Multicast Routing, IPv6 Unicast Routing, Ingress and Egress Policing, Egress Shaping, SRR, WRED, 802.1Q and ISL support, Multiple SPAN sessions, RSPAN, Integrated packet buffer, External TCAM, uRPF, StackWise Plus (64G stack), SGT capability, IPv6 Multicast Routing (wide keys), Support for Jumbo Frame Routing (9216), Support for multiple First Hop Router Redundancy protocols at once, Hardware Merge TCAM, Integrated Hash Tables, Integrated associated data tables, Support for MadMax ASIC (Fabric with 4 stack ports), Support for Local Switching, FlexStack support, Low power -> Fanless possible, MACSec, ERSPAN, COPP …


# Catalyst 4500



# K1

Sup1

2000


# K2

Sup3

2002


# K5

Sup6E

2007

90nm

600M Transistors


# K10

Sup7

2010

90nm

1.2B Transistors


Catalyst

4000/4500

ASIC Innovation

# Catalyst 4000/4500 ASIC Innovation

High-performance centralised switching – 492 Gbps L2 / L3 capacity, IPv4 and IPv6 forwarding in hardware, up to 250 Mpps Multicast, up to 60Gbps Recirculation bandwidth, 256K routes (128K IPv6) and 48K adjacencies, ECMP routing, Unicast RPF (strict and loose), VRF-lite (64 VRFs), EVN support, 64K input and 64K output ACEs, 8 bidirectional SPAN sessions, NetFlow (up to 128K flows), Advanced Congestion Avoidance: Dynamic Buffer Limiting (DBL), Smooth Round Robin (SRR) with sharing and shaping per queue, Granular per-port per-VLAN policies, IP Source Guard, 64 CPU queues with CoPP, large (32MB) high performance shared packet buffer, PVLAN support for promiscuous and isolated trunks, 1:1 & 1:N VLAN Translation, Packet & byte counters per adjacency, Policy-based Routing …


# Catalyst 6500 6800


| Cat 5000 Sup1 | Cat 5000 Sup2 | Cat 5500 Sup3 | Cat 6000 Sup1 | Cat 6500 Sup1A | Cat 6500 Sup2 250nm 24M Trans | Cat 6500 Sup720 3A/B/BXL 180nm 100Trans | Cat 6500 Sup720 3C/XL 130nm 102M Trans | Cat 6500 Sup2T Nexus 7000 45nm 1.4B Trans |
|---|---|---|---|---|---|---|---|---|

# Catalyst 5000 / 5500 / 6000 / 6500 / 6800
# Nexus 7000

# Catalyst 5000/6500 ASIC Innovation

IPv6 Unicast + Multicast in Hardware, RSPAN, ERSPAN, GOLD, OBFL, ACL Merge Optimisation, Netflow, MPLS in Hardware, IGMPv3, EoMPLS, VPLS, A-VPLS, NAT, PAT, RBACL, Egress Multicast Replication, Full and Sampled Netflow, Ingress/Egress Netflow, IPv4 Tunnelling, GRE, IPv6 Tunnelling, 6to4 Tunnelling, ISATAP Tunnelling, Recirculation, Bridge Domains, Static MAC match conditions, Virtual Switch Link, Bi-Directional PIM, Control Plane Policers, HW Rate Limiters, Ingress/Egress Aggregate Policers, Microflow Policers, VSS support, Strict and Loose RPF Check, HW PIM Register Encap/Decap, MPLS QoS, Ingress/Egress DSCP Mutation, QPPB, SGT, 3 Colour Policing, MLD Snooping, RBH for Etherchannel Mapping, Port Security, Optimised IP Multicast Flooding, 16 Way ECMP …


# AGENDA

- Why ASICs?
- How is an ASIC developed?
- Merchant vs. Custom
- Cisco ASIC History
- The Move to Programmability
- QFP
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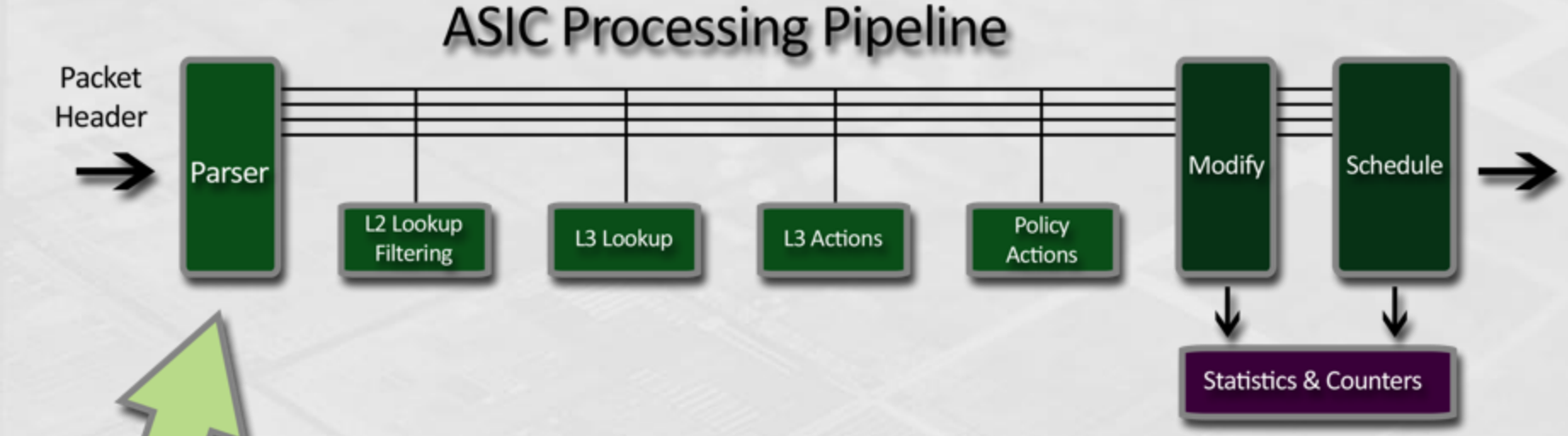
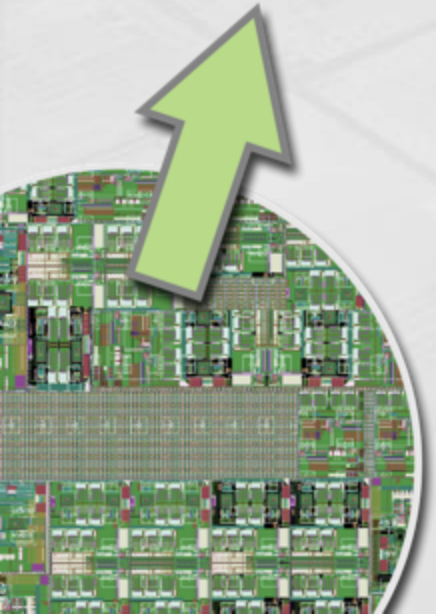
- Summary



# Traditionally the pipeline is FIXED


**Clean Slate**

**SDN Ground Zero**

SDN

OPENFLOW

OVERLAYS

ASICs

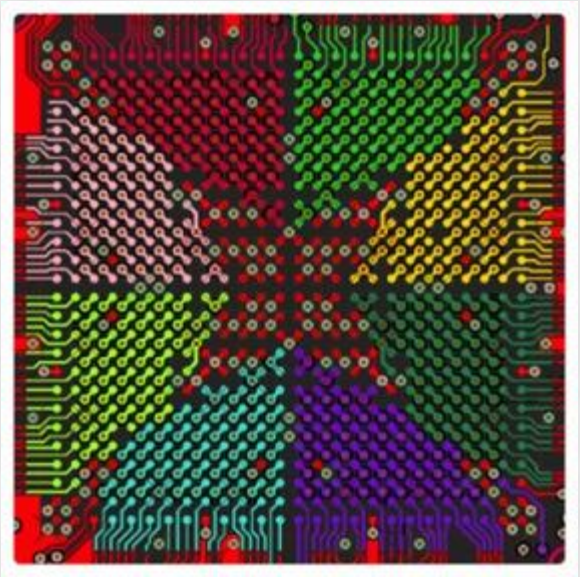
ORCHESTRATION

AND MORE

# What is the most programmable silicon available today?

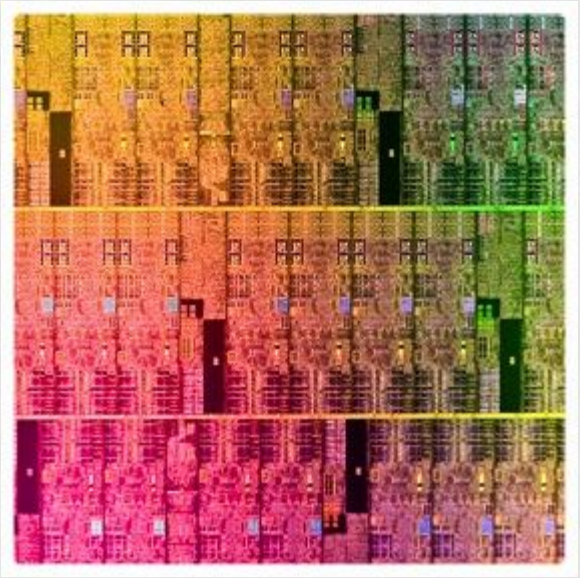

# The General Purpose CPU…

# Very Flexible BUT SLOW…



# Field Programmable Gate Array (FPGA)

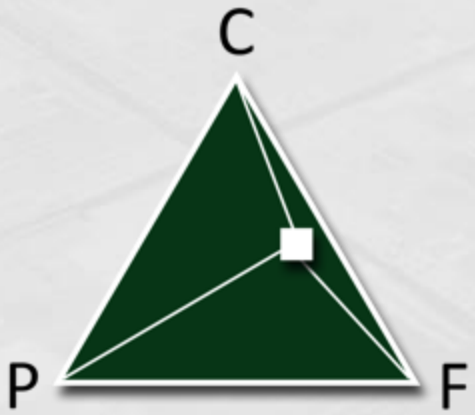
Flexible
And Faster
But Costlier…



The Network ASIC …

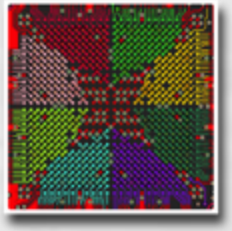
Very Fast BUT FIXED…

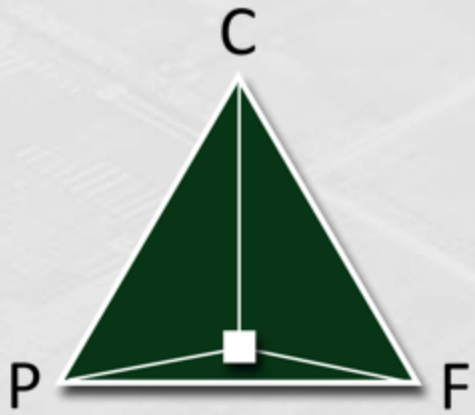
## Traditional CPU


COST ~
PERFORMANCE
FLEXIBILITY ✓

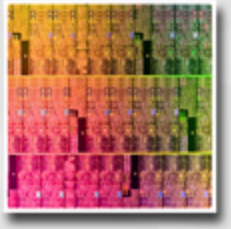
## FPGA

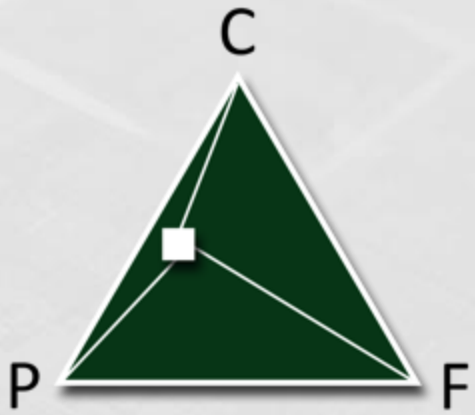





COST
PERFORMANCE ✓
FLEXIBILITY ✓

## Network ASIC

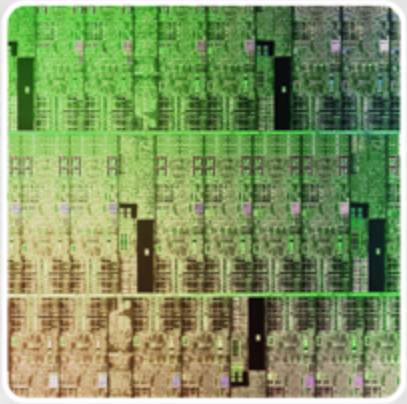


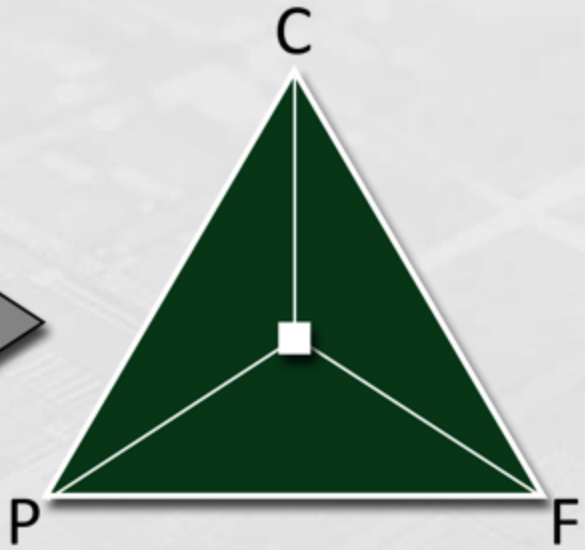



COST ✓
PERFORMANCE ✓
FLEXIBILITY

# So where can Programmable ASICs help us?

Programmable ASIC






COST ✓

PERFORMANCE ✓

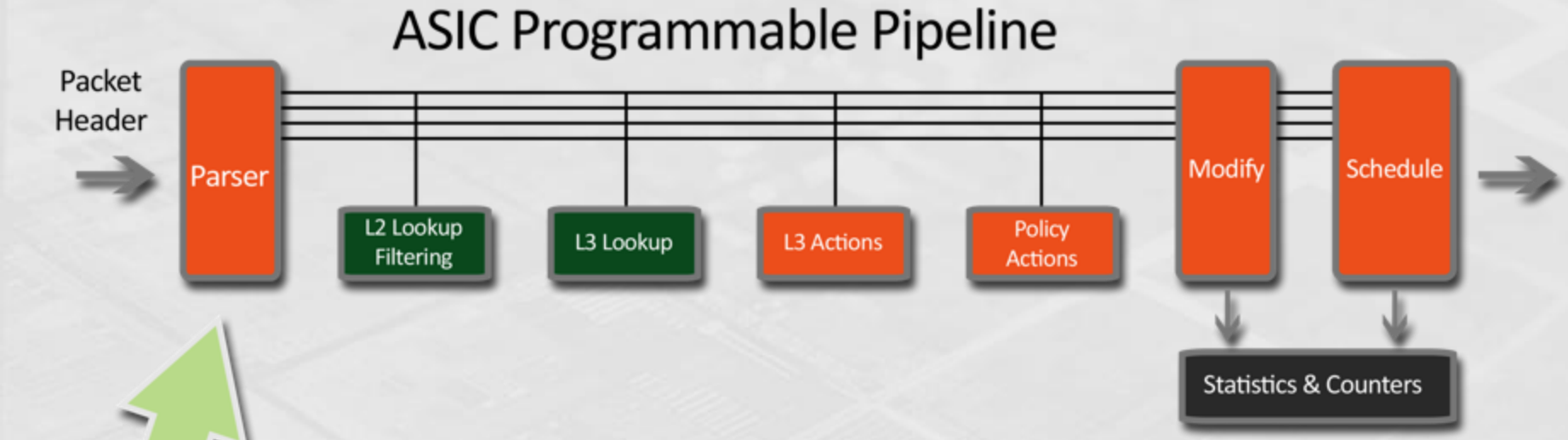
FLEXIBILITY ✓

# Programmability introduces flexible pipelines…

ASIC Engineer

Microcode Update

New ASIC Functionality




# Modify processing behaviour without incurring re-spin

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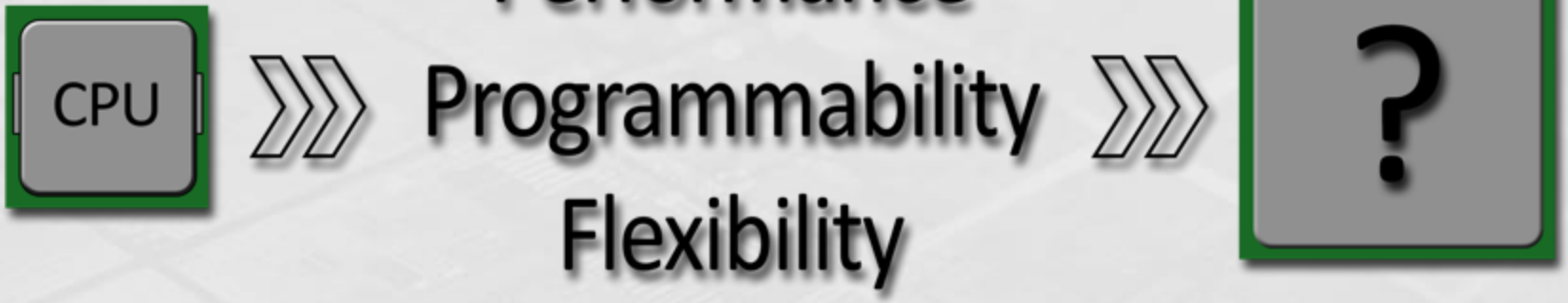
# Programmable Routing Silicon –

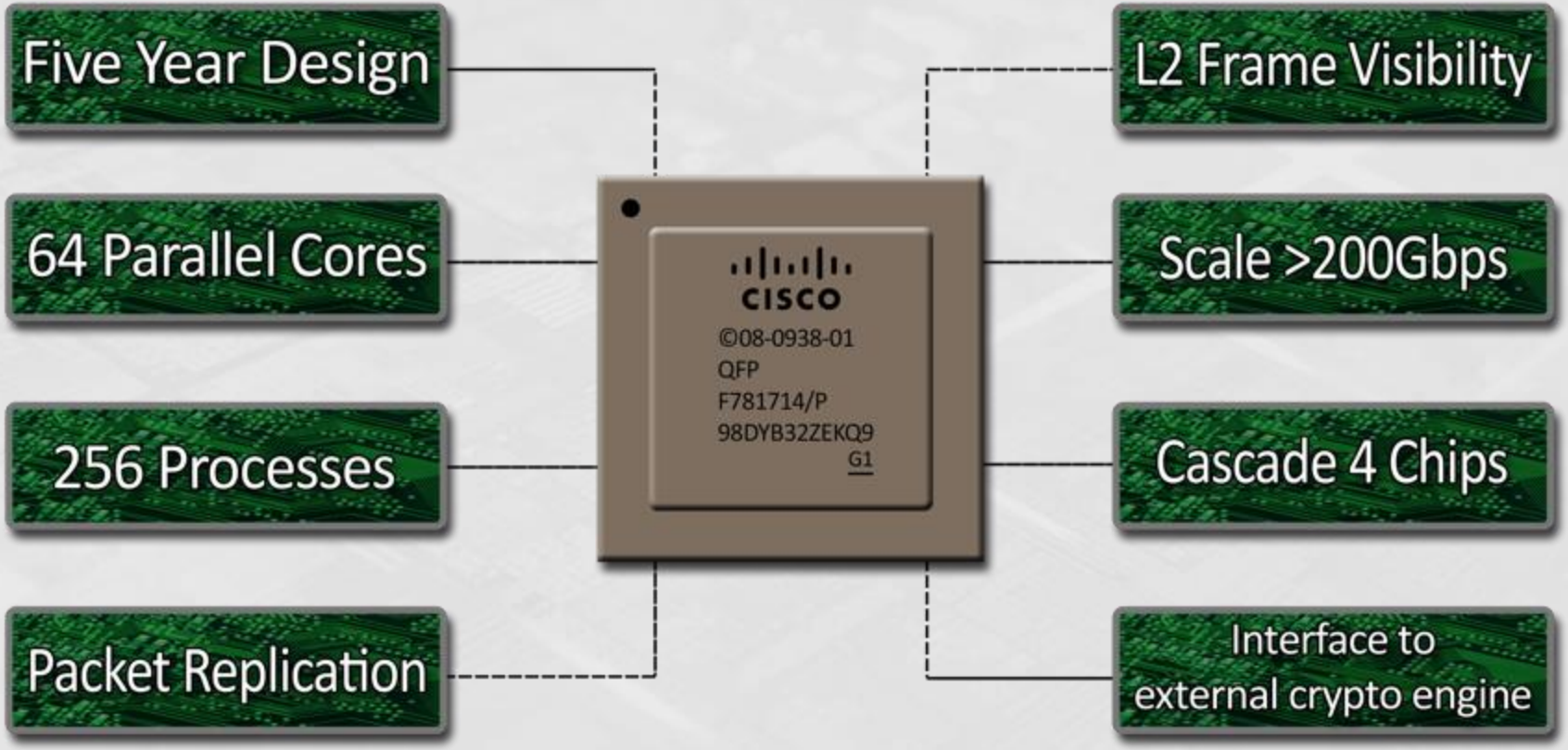
# Quantum Flow Processor QFP



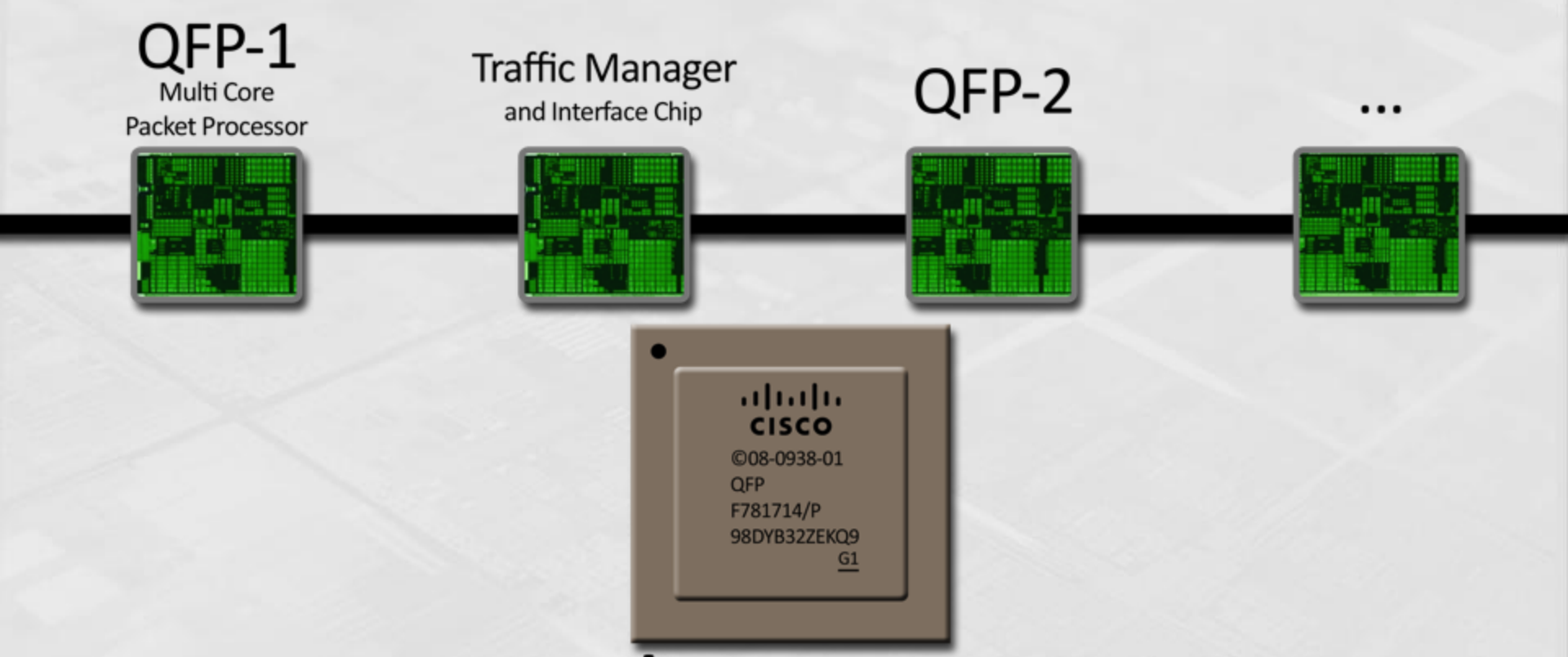

# Evolution of Routing


QUANTUM FLOW PROCESSOR (QFP)

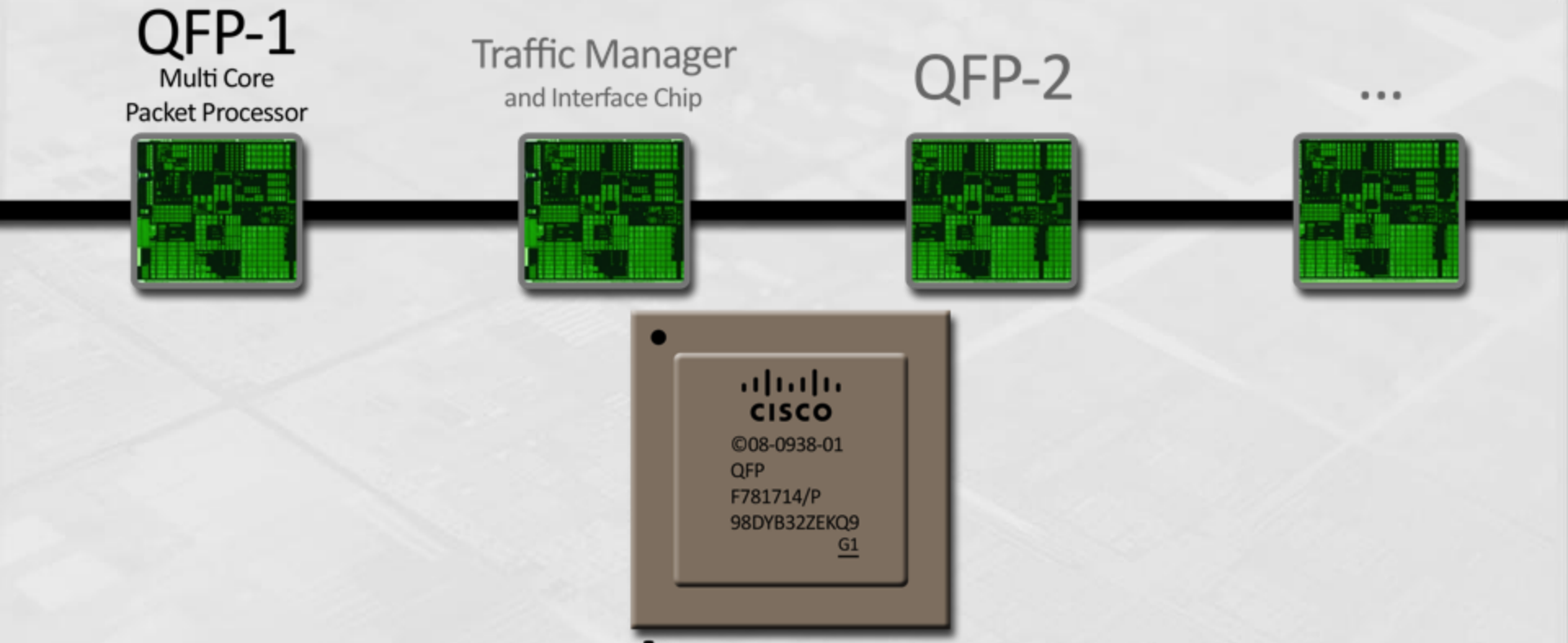
- High Performance
- Programmable
- Feature Rich
- Price/Performance
- Longevity/Flexibility



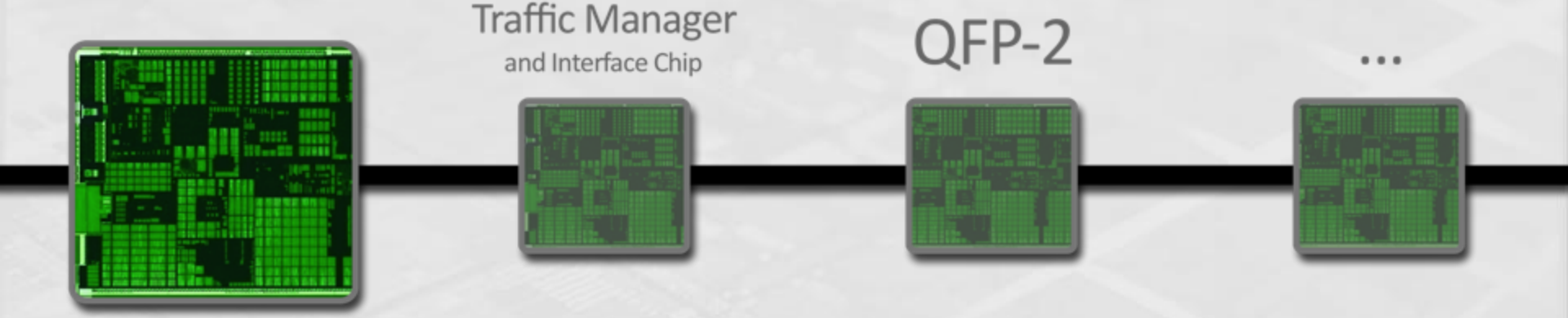

## 100% Developed Cisco Networking Silicon




# QFP Development History




# QFP Development History




# QFP-1

## Multi Core Packet Processor

1.2 GHz / 400 MHz

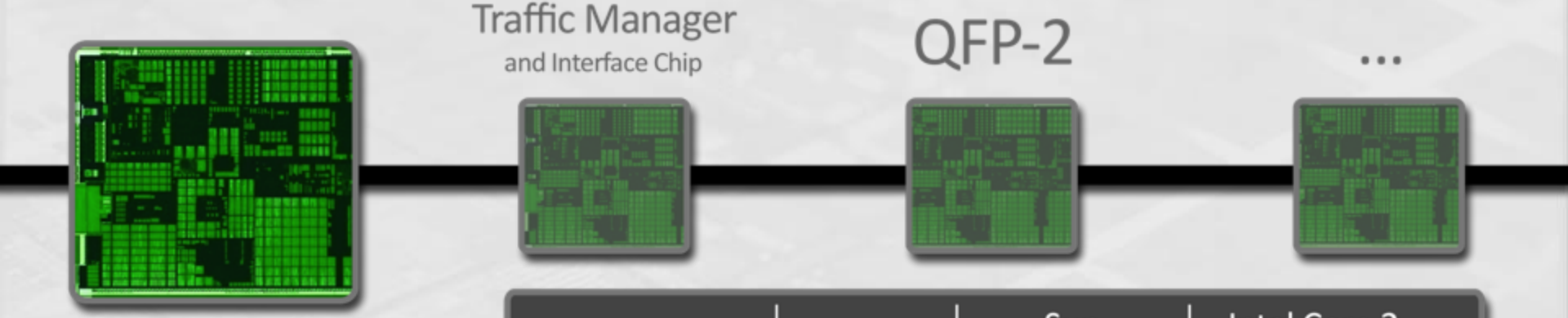
40 custom multi-threaded CPUs

90nm, 8-layers metal

382 $mm^2$

307 million transistors

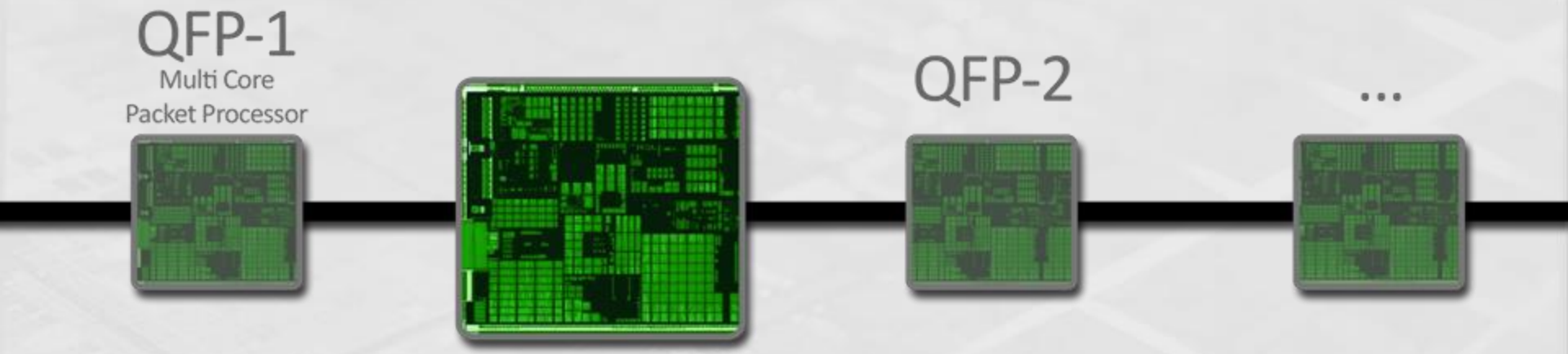
1019 I/O, including 800 MHz DDR




# QFP-1

Multi Core
Packet Processor

| | Cisco QFP | Sun Ultrasparc T2 | Intel Core 2 Mobile U7600 |
|---|---|---|---|
| Total # Processes (Cores x Threads) | 160 | 64 | 2 |
| Power per Process | 0.51w | 1.01W | 5W |
| Scalable traffic management | Queues | None | None |




# Traffic Manager

## & Interface Chip

400 MHz

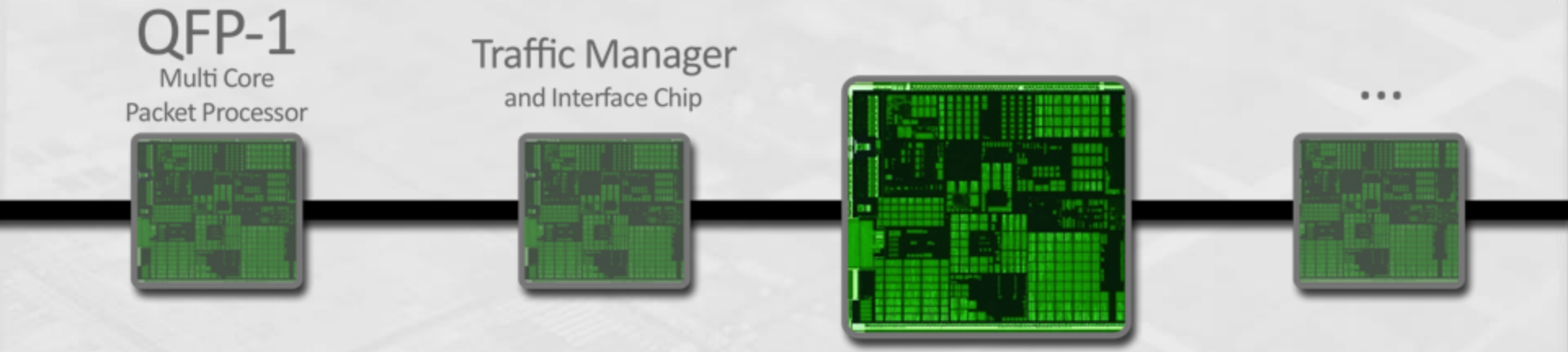
Buffering, 128K queues
Hardware HQF scheduling

90nm, 8-layers metal

332 $mm^2$

522 million transistors

1318 I/O, including
800 MHz DDR




# QFP-2

1.2 GHz / 400 MHz

64 custom multi-threaded CPUs

Up to 1500 MHz Buffering, 116K queues

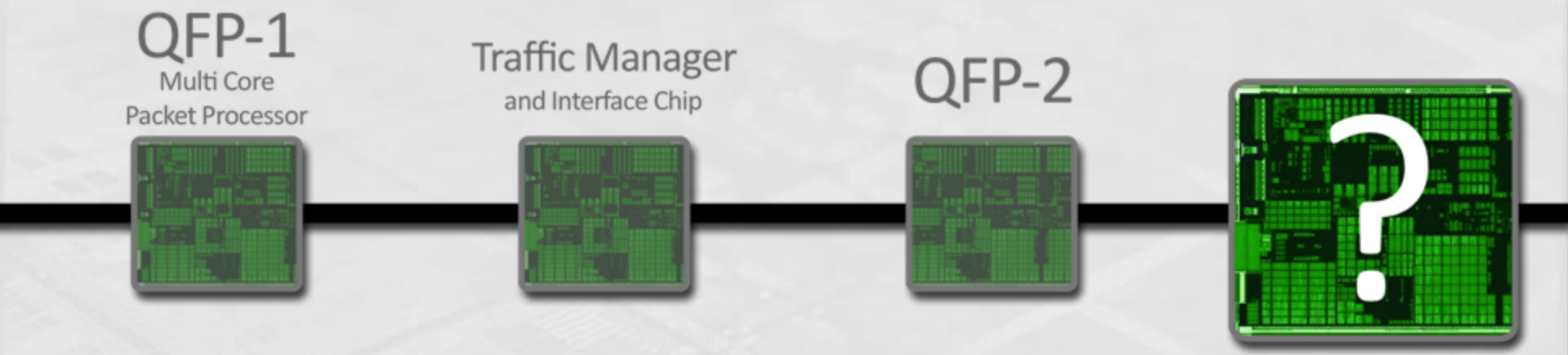
Hardware HQF scheduling

40nm, 10-layers metal

324 sq mm

1.8 Billion transistors

1480 I/O, including 800 MHz DDR




# More to Come

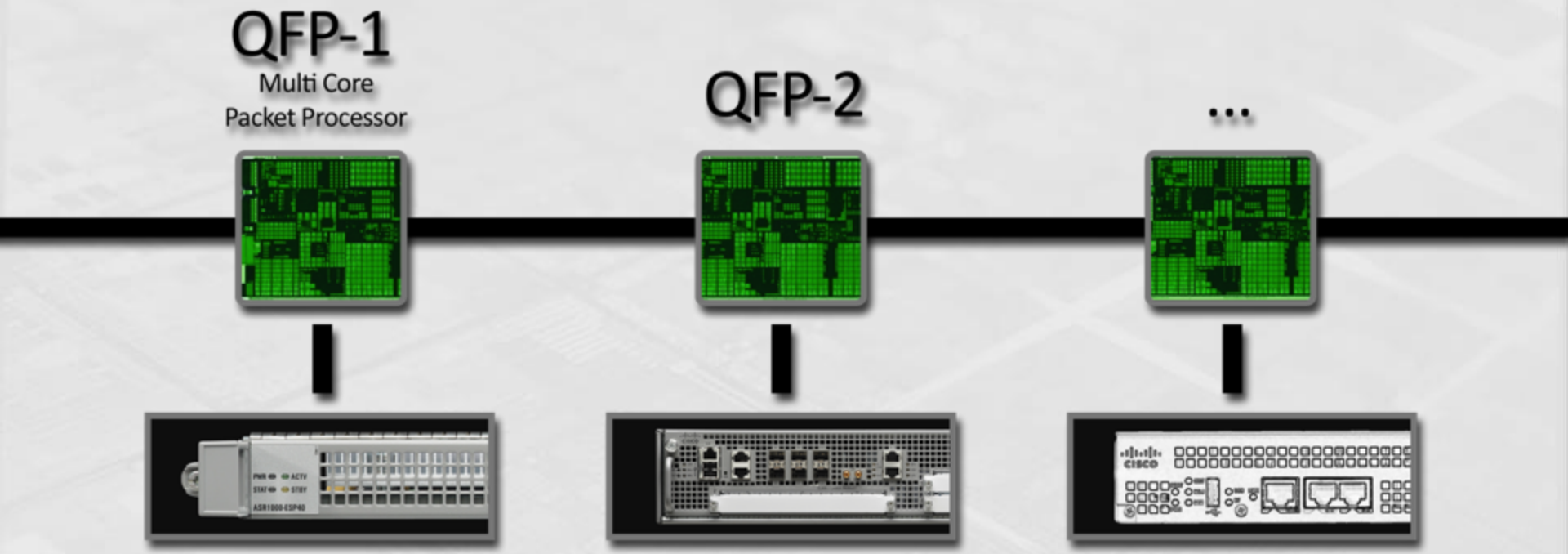

# What does this mean for me?

# QFP Programmable Hardware

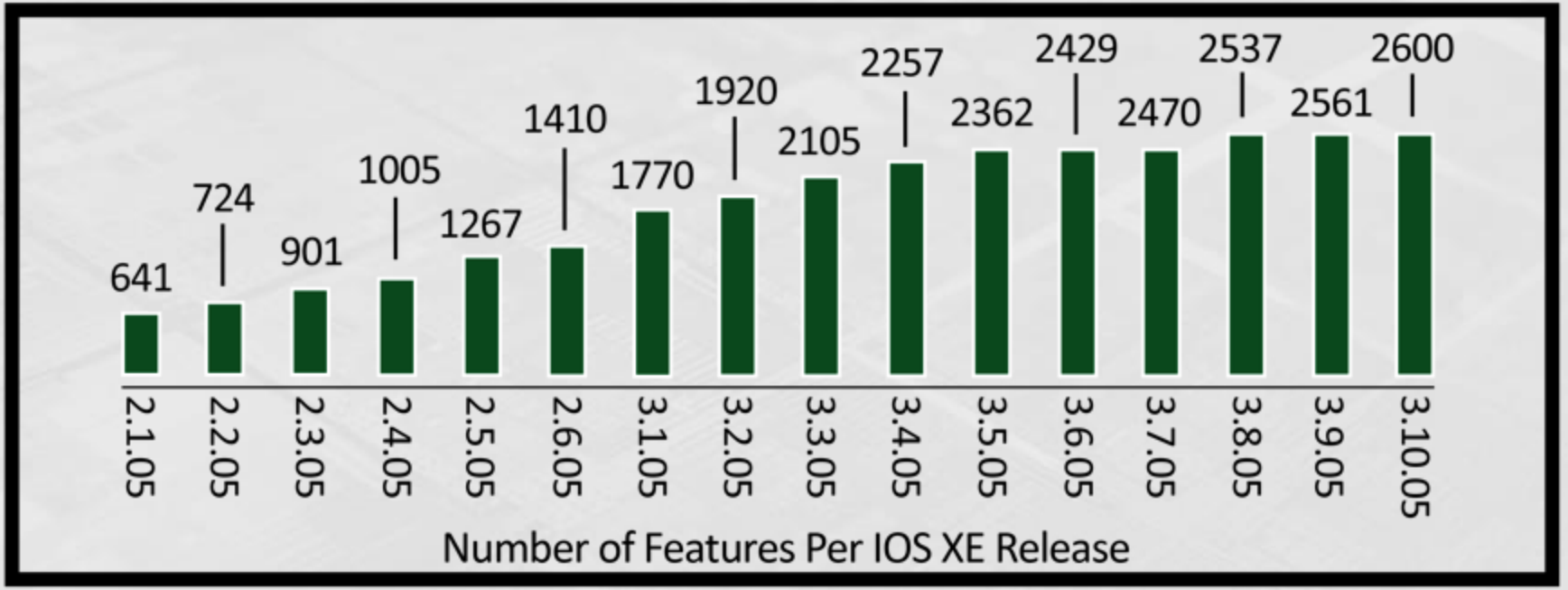
# equals

# FLEXIBILITY
# PERFORMANCE

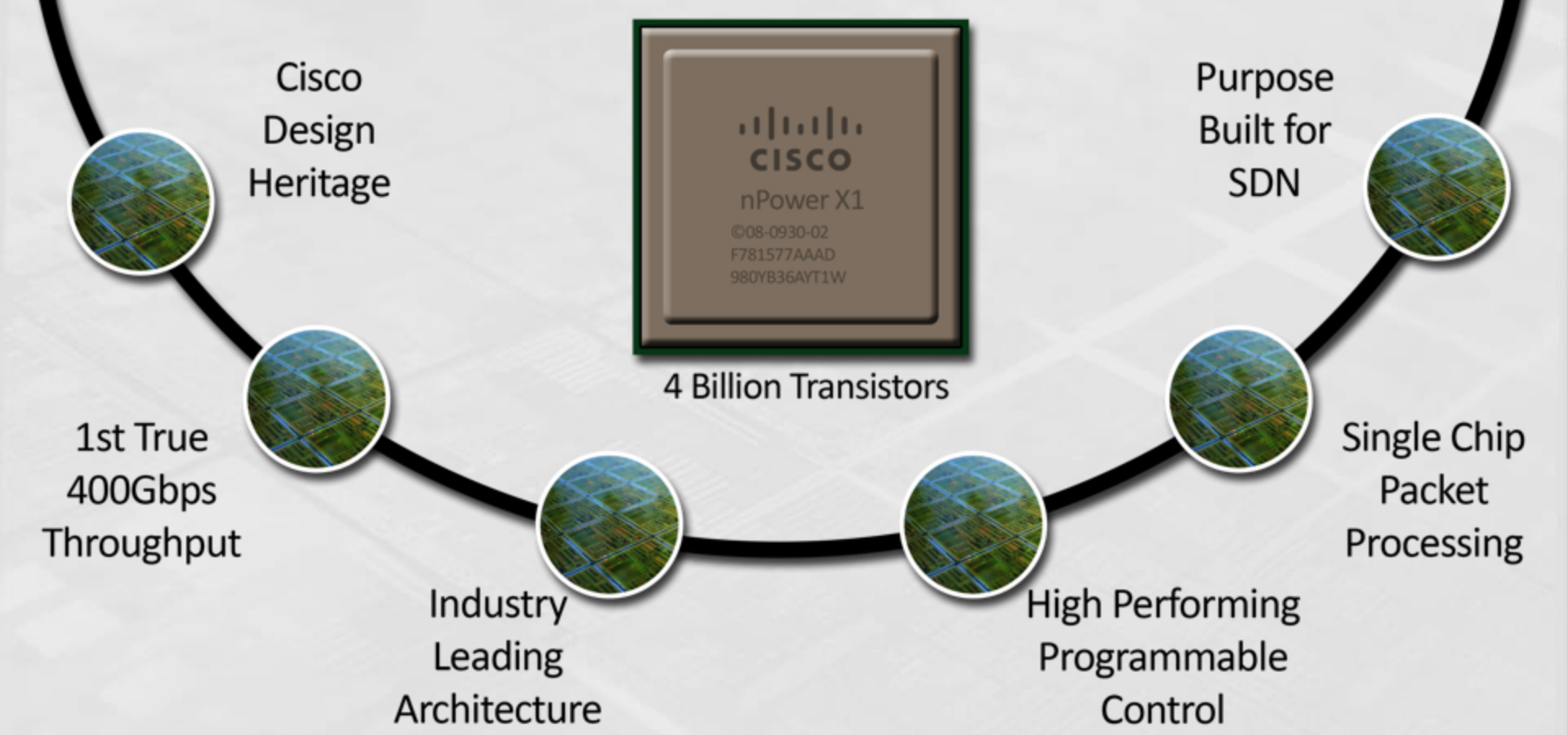
# QFP Platforms



# QFP Feature Velocity




Over 2600 features




# Next-Gen Network Processor - nPower X1

# AGENDA

Why ASICs?
How is an ASIC developed?
Merchant vs. Custom
Cisco ASIC History
The Move to Programmability
QFP
UADP
Summary

# Programmable Switching Silicon –

# Unified Access Data Plane UADP

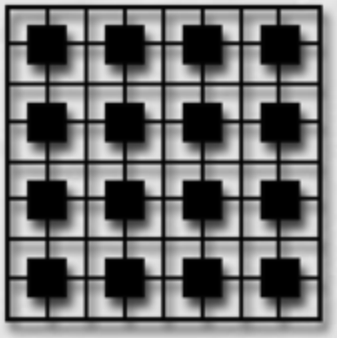

# UNIFIED ACCESS DATA PLANE (UADP)

1 2 3 4 5

# 5 Key Capabilities


# UNIFIED ACCESS DATA PLANE (UADP)

1 2 3 4 5



Microcode Programmable Pipeline w/Flexparser

# UNIFIED ACCESS DATA PLANE (UADP)


Stack Master

Stack Member

Stack Member

240G
Stacking Interface
integrated into ASIC

UNIFIED ACCESS DATA PLANE (UADP)



On Chip Micro Engines
Fragmentation / Reassembly, Encryption / Decryption (AES-128, CBC)

# UNIFIED ACCESS DATA PLANE (UADP)



High-Performance Recirculation Path (less than 1usec Recirculation Latency)

# UNIFIED ACCESS DATA PLANE (UADP)



Integrated On Chip
Netflow
24K Entries

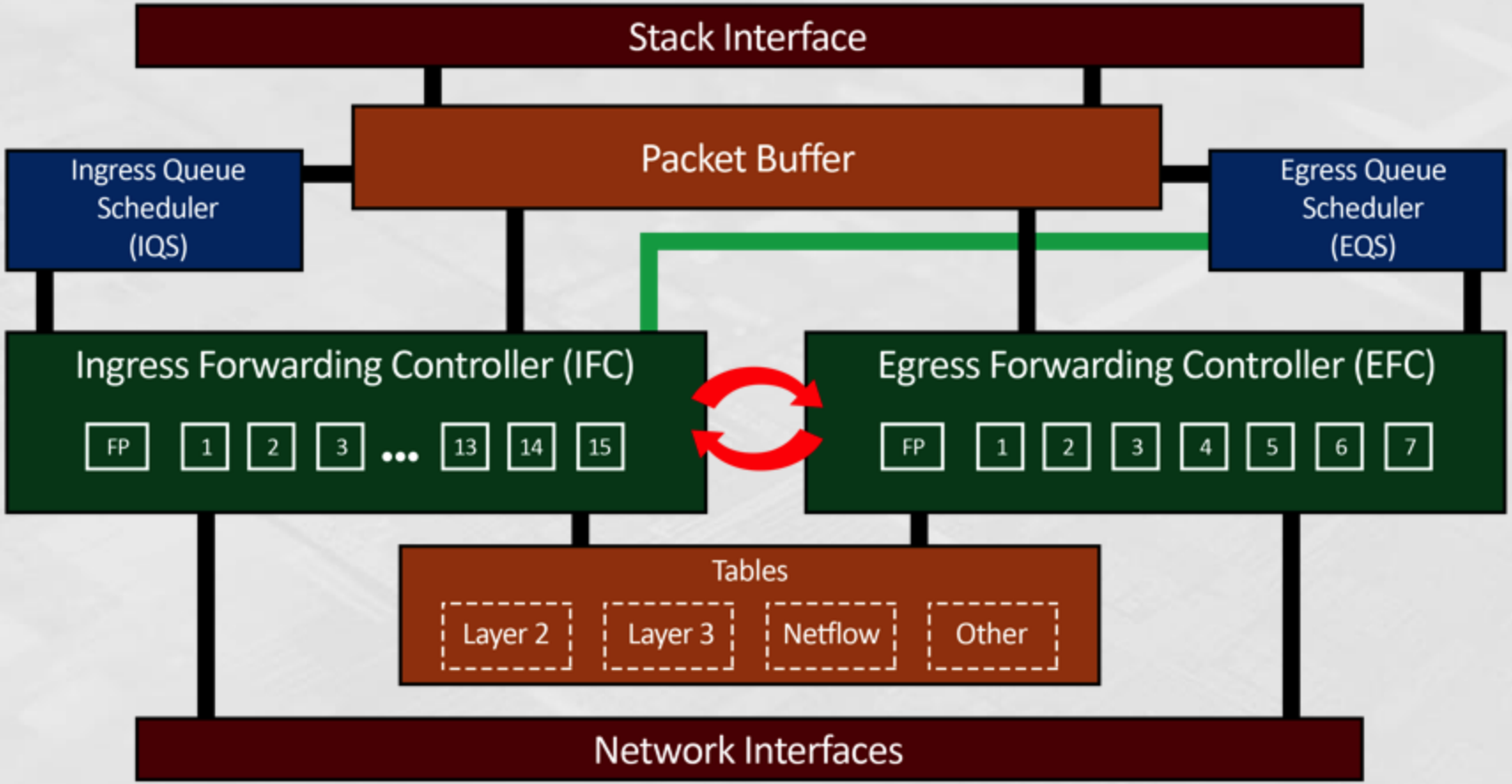
# UNIFIED ACCESS DATA PLANE (UADP)


Stack spatial reuse | Local switching | Jumbo frames | 8 egress queues per port | Dynamic fair buffer sharing | Active queue management | WRED | Approximate Fair Drop | Per Flow counters | Control Plane Protection | SRR scheduling | Microflow 1R2C policers | Aggregate 2R3C policers | Policer chaining | Class-based flow control | Packet parser | Unicast RPF | Private VLANs | PBR | IGMP / MLD snooping | SGT support | Role-based ACLs | Policy-based ACLs | Client-based or Group-based ACLs | L2 / L3 tunnel support | CAPWAP | DTLS | sRTP | Embedded logic analyser | SPAN, RSPAN, ERSPAN, Flow SPAN …

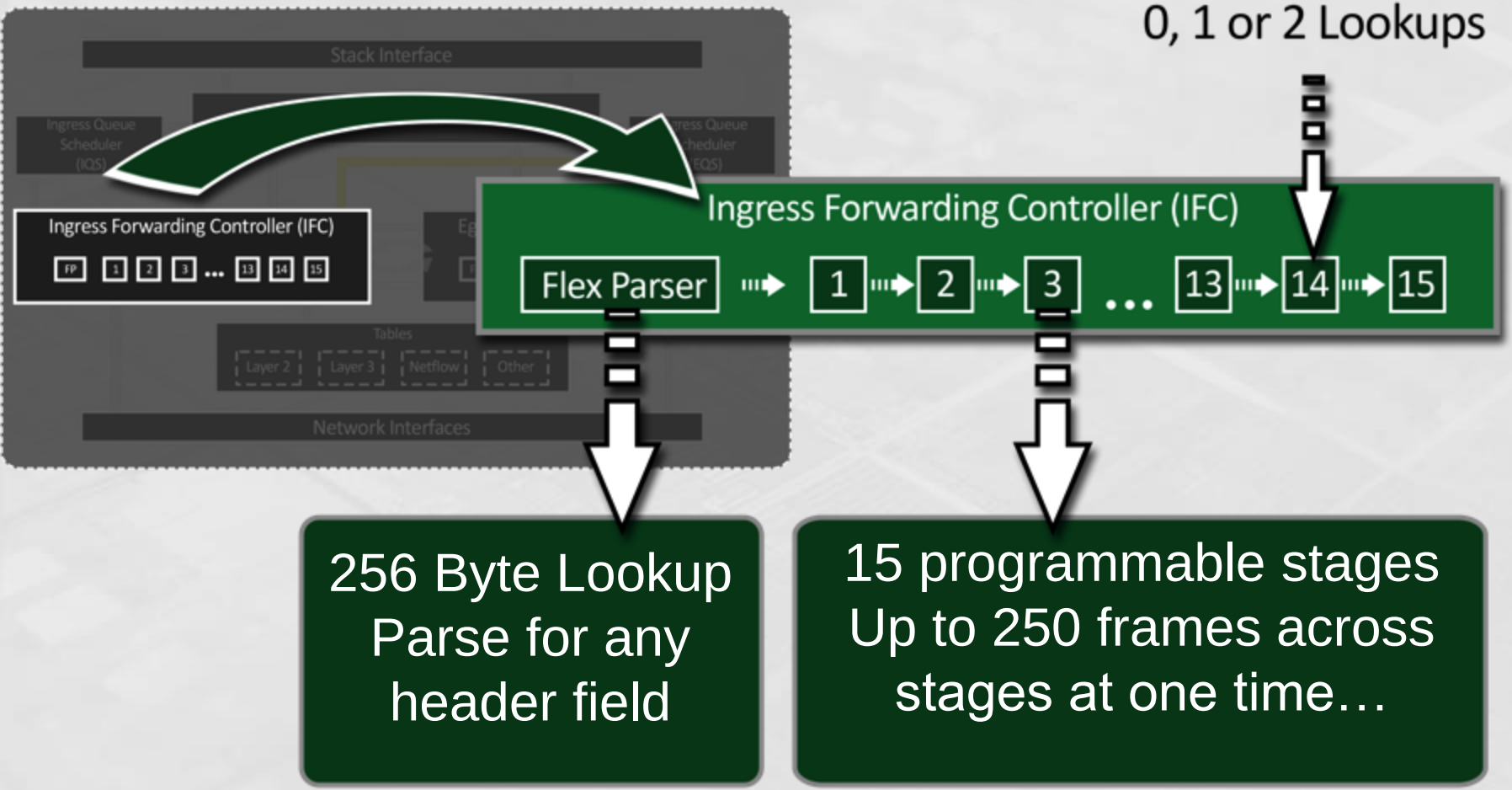
*Features noted are hardware capable with UADP, but are not yet necessarily productised*

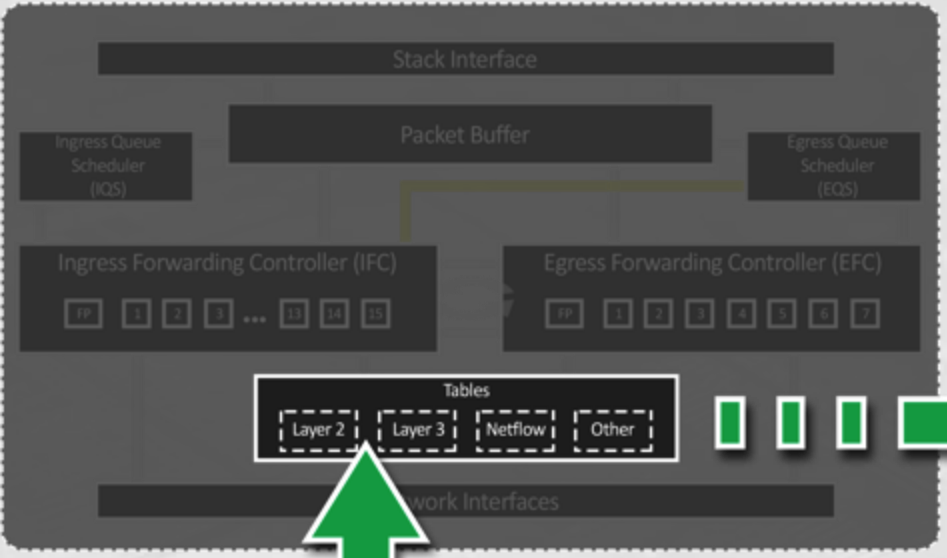
# UNIFIED ACCESS DATA PLANE (UADP)

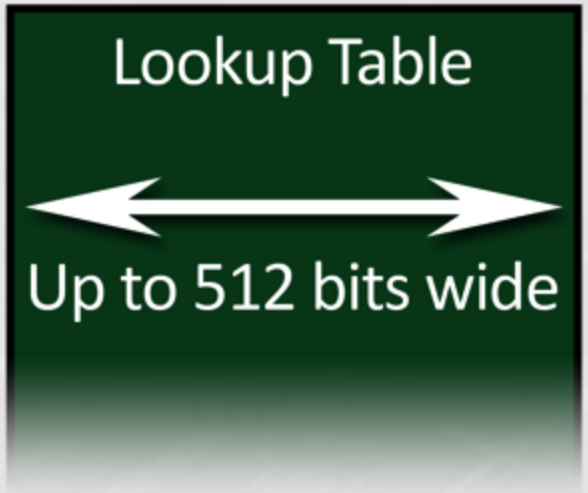
# Let’s look at UADP more closely…




# Unified Access Data Plane (UADP) Fuctional Diagram

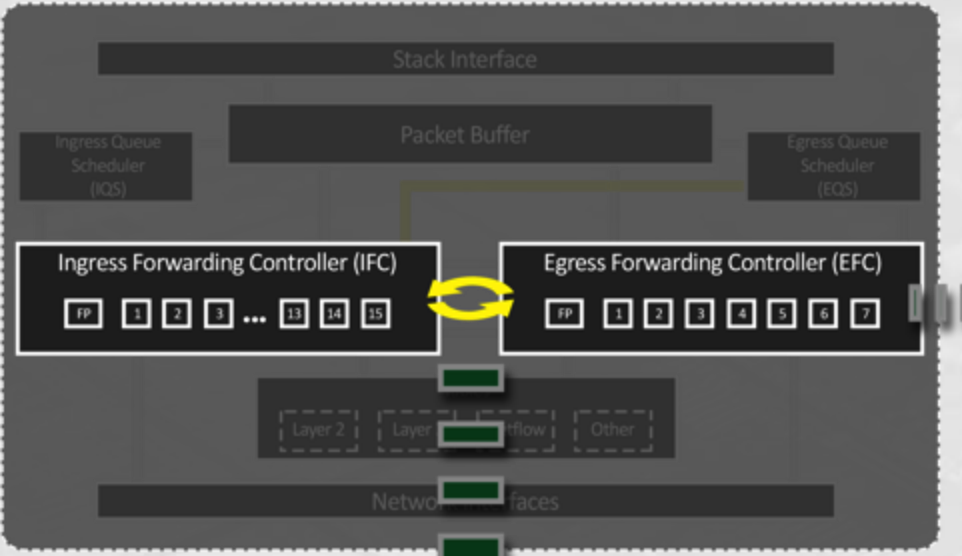





All Tables On-Chip

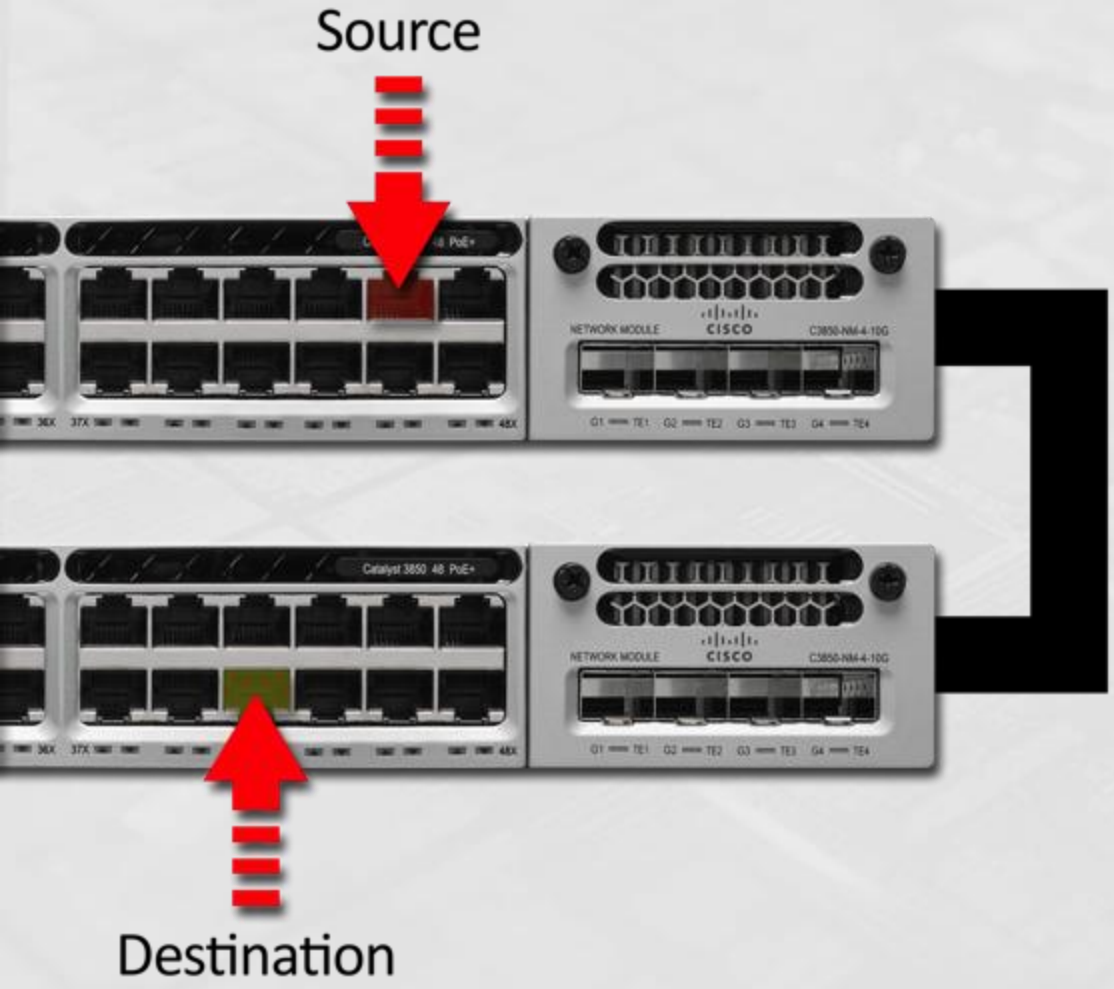
# Tb of On-Chip Bandwidth



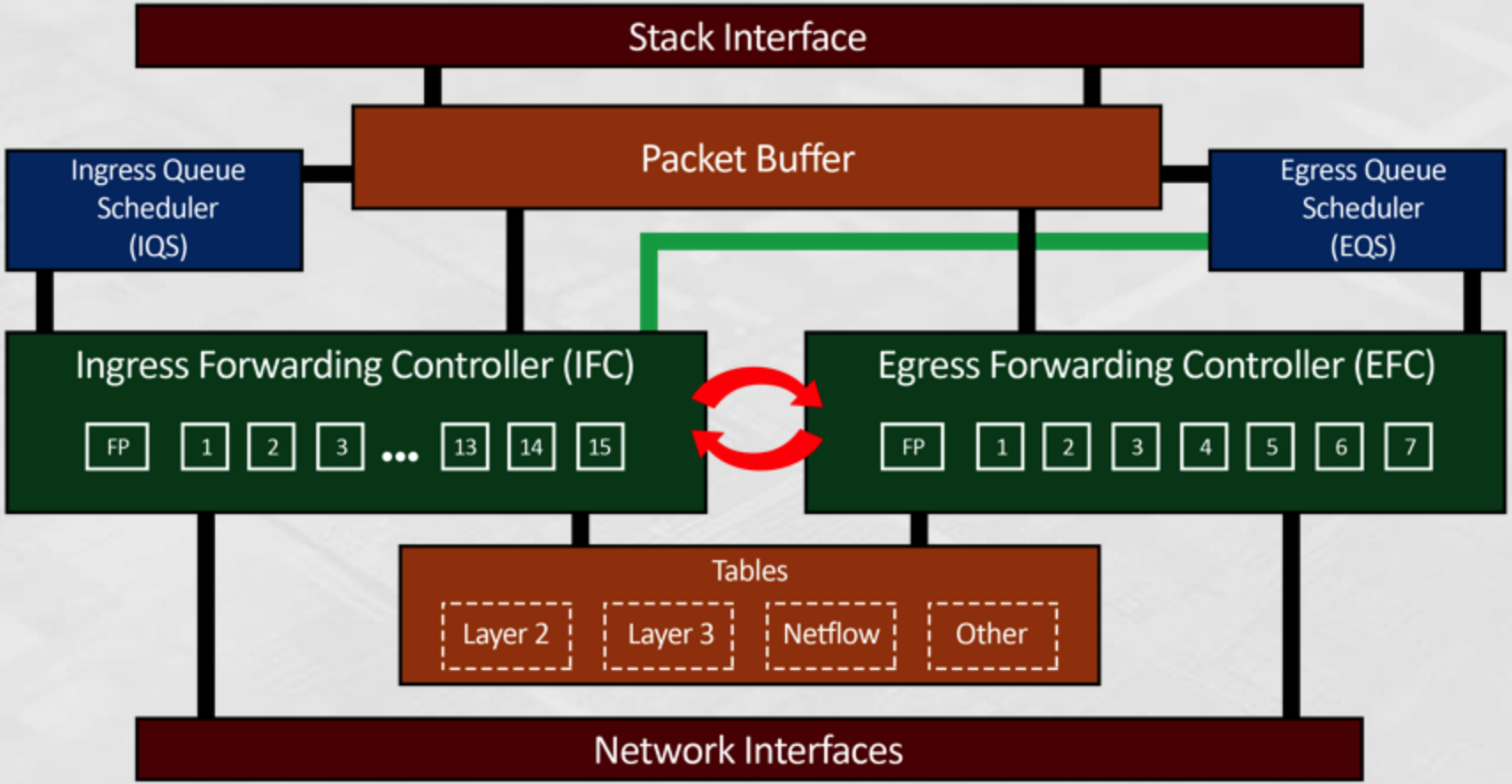


Re-Circulation

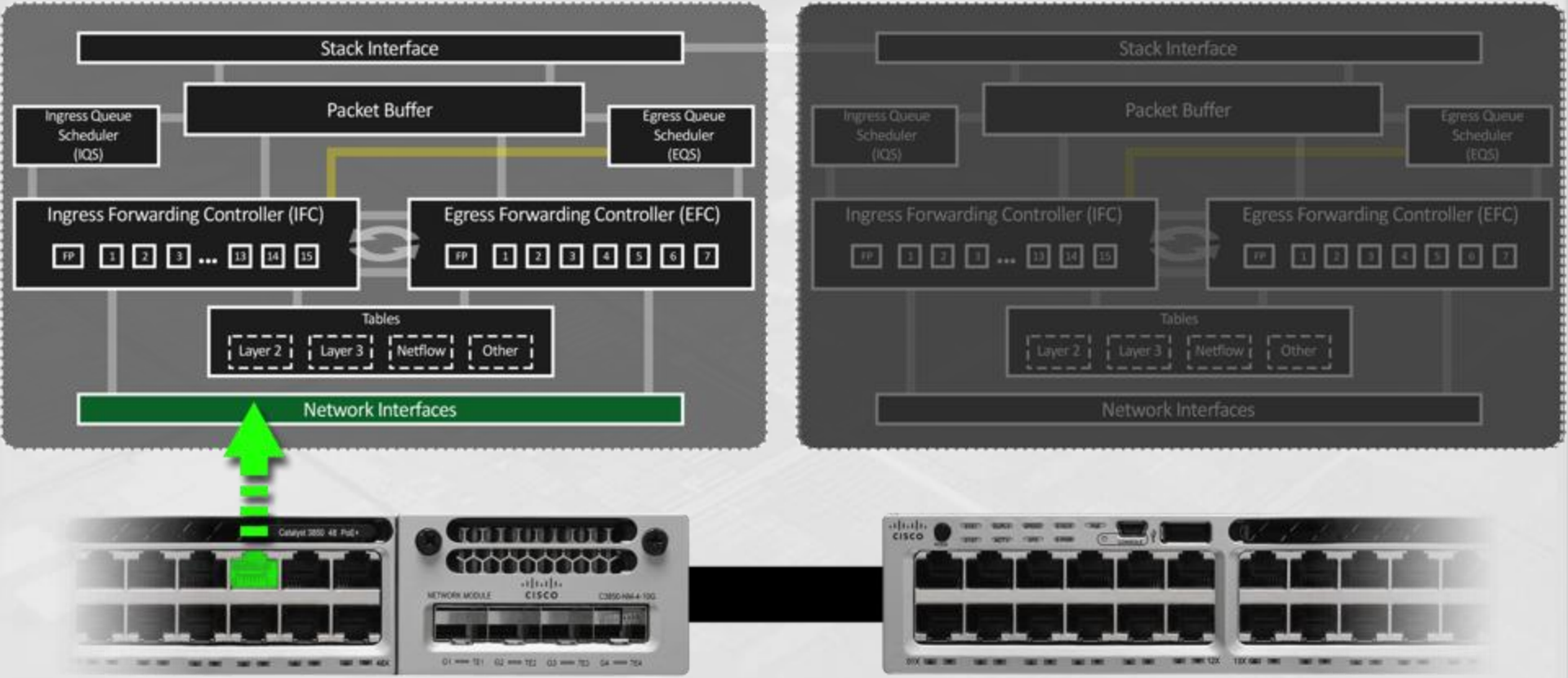
Recirculate up to 16 Times

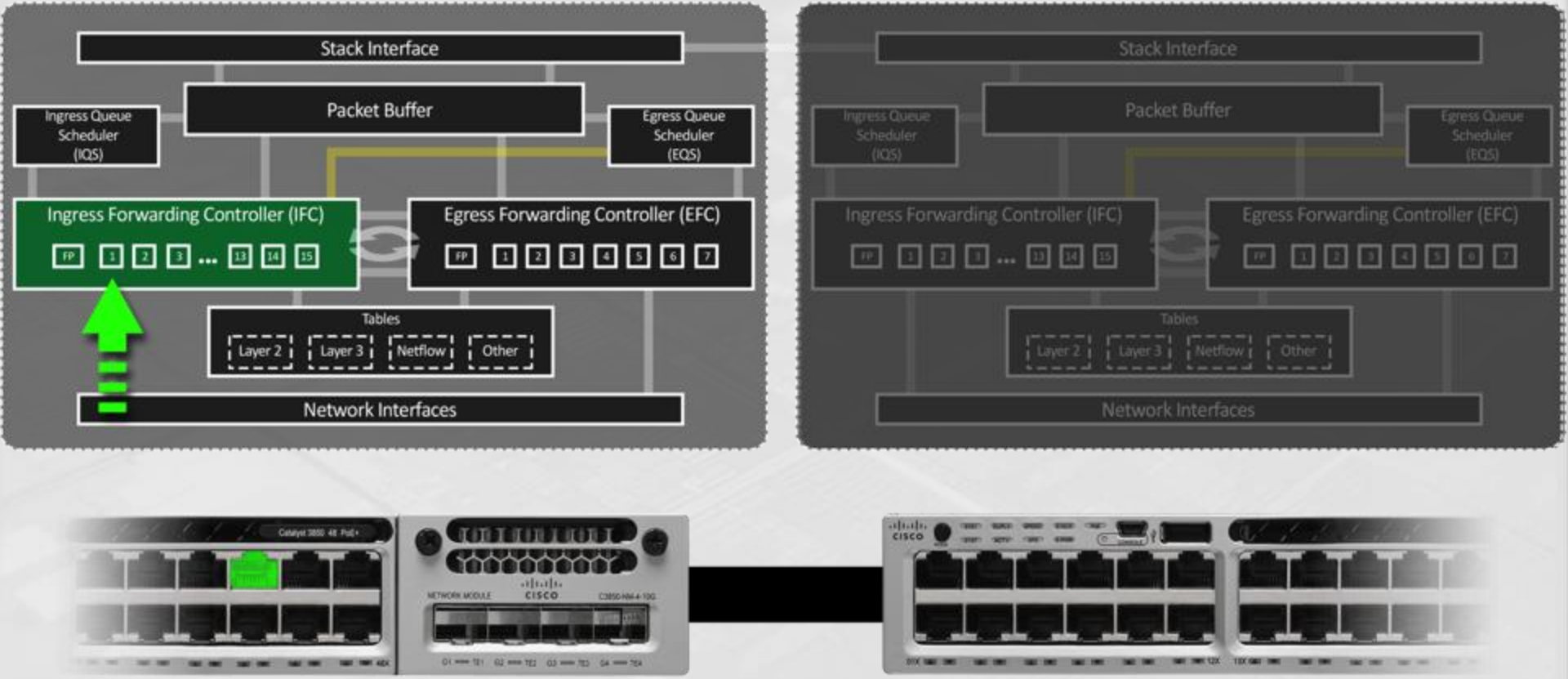


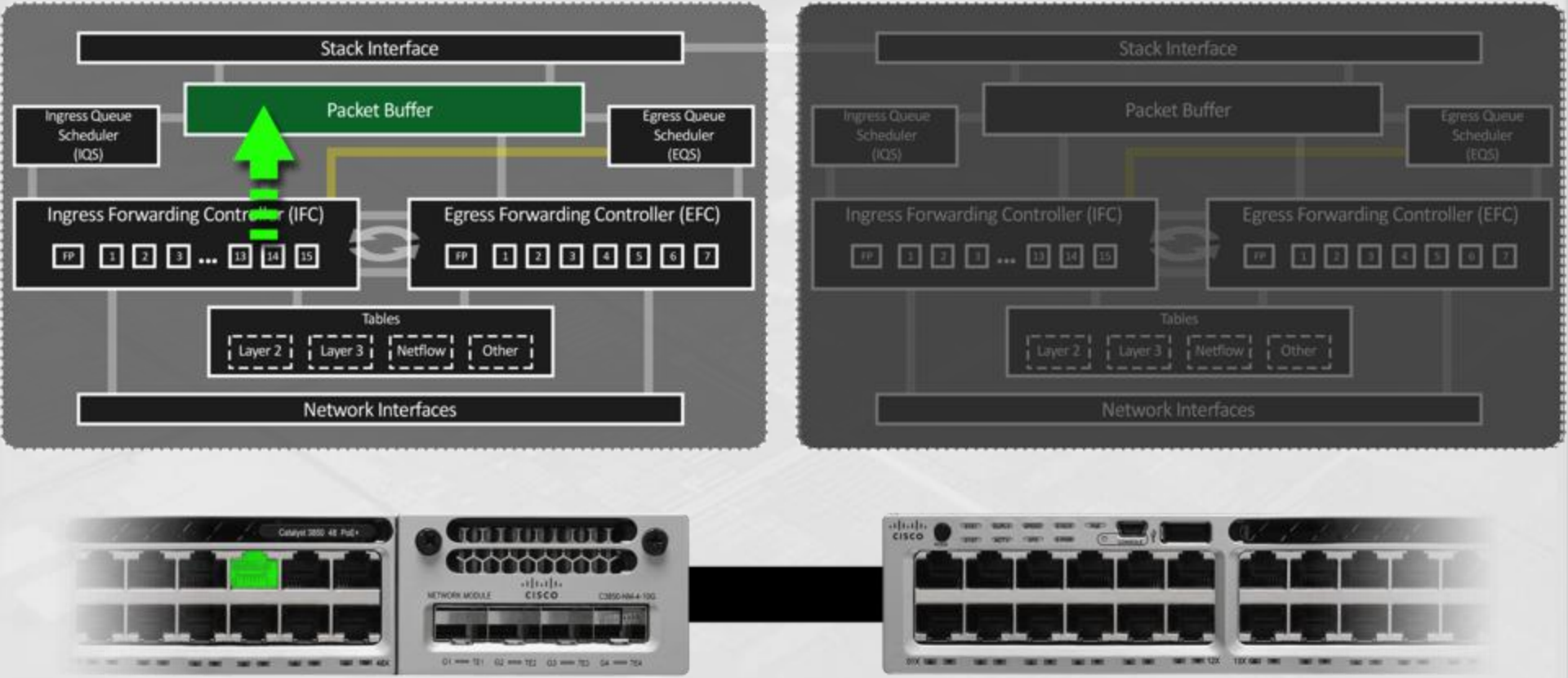

# UADP Packet Walk Scenario

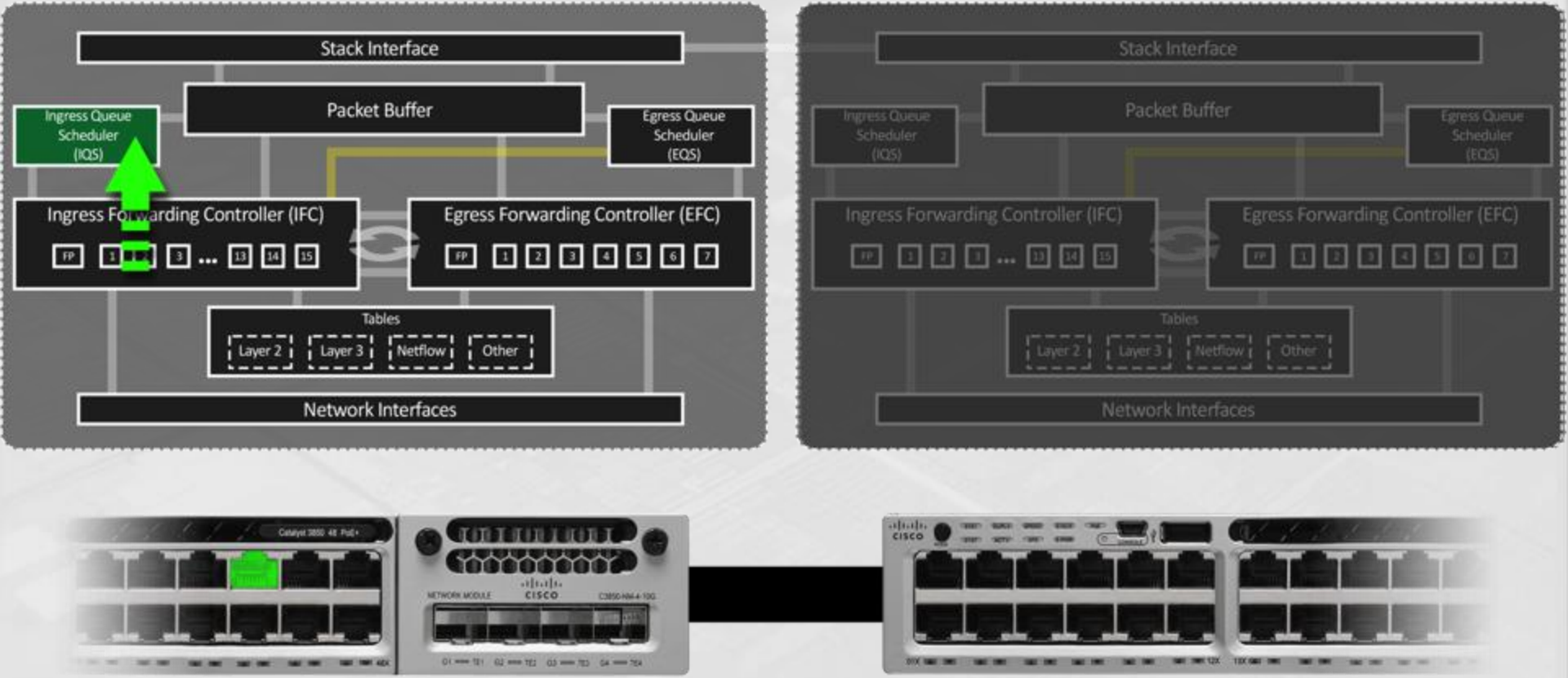


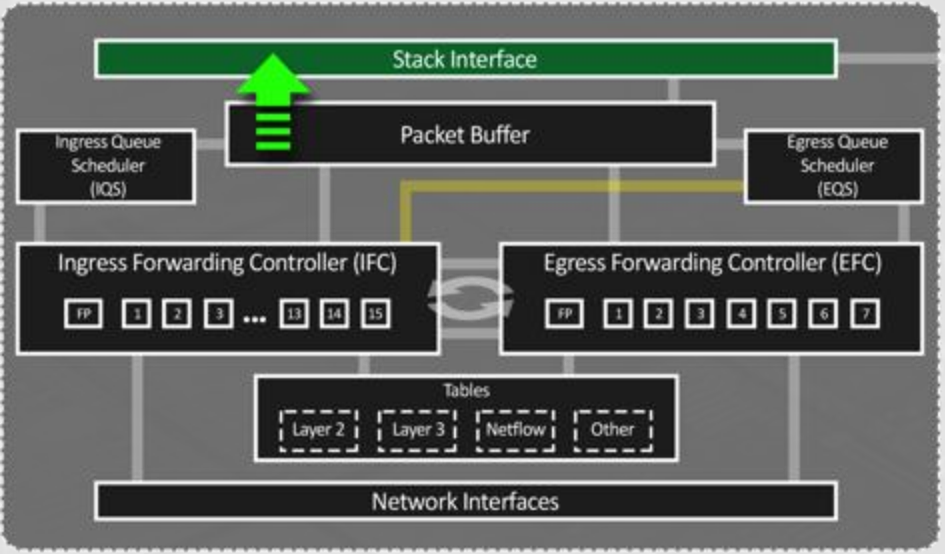

# Unified Access Data Plane (UADP) Fuctional Diagram

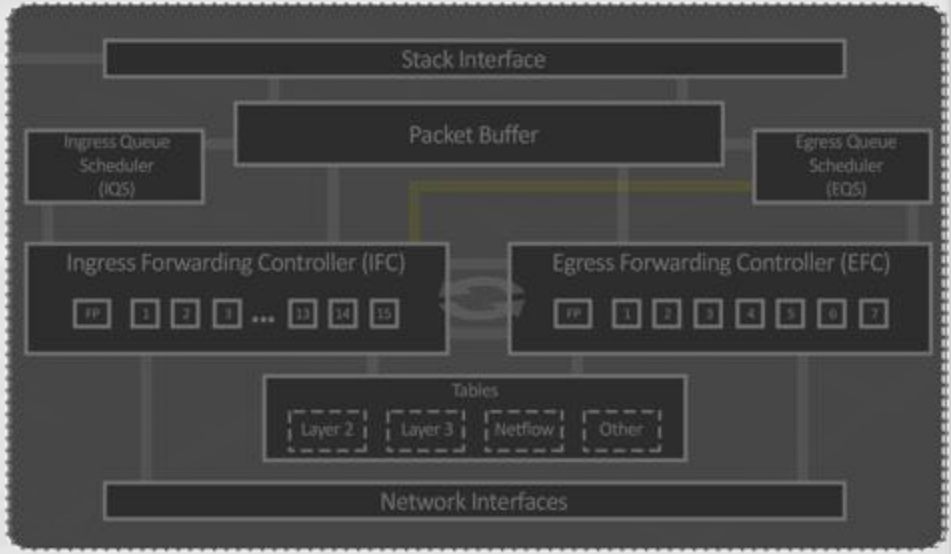


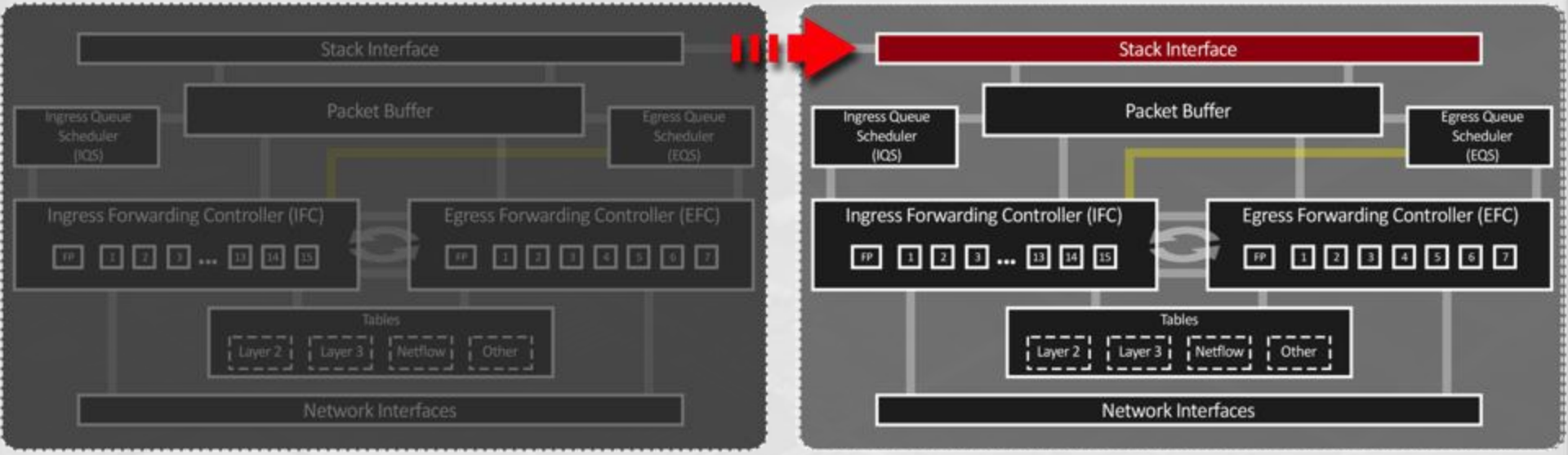


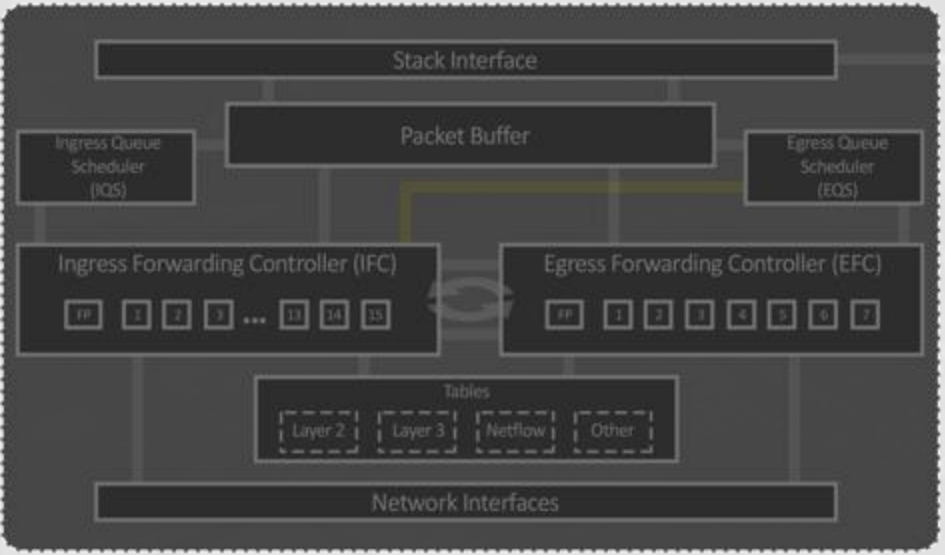


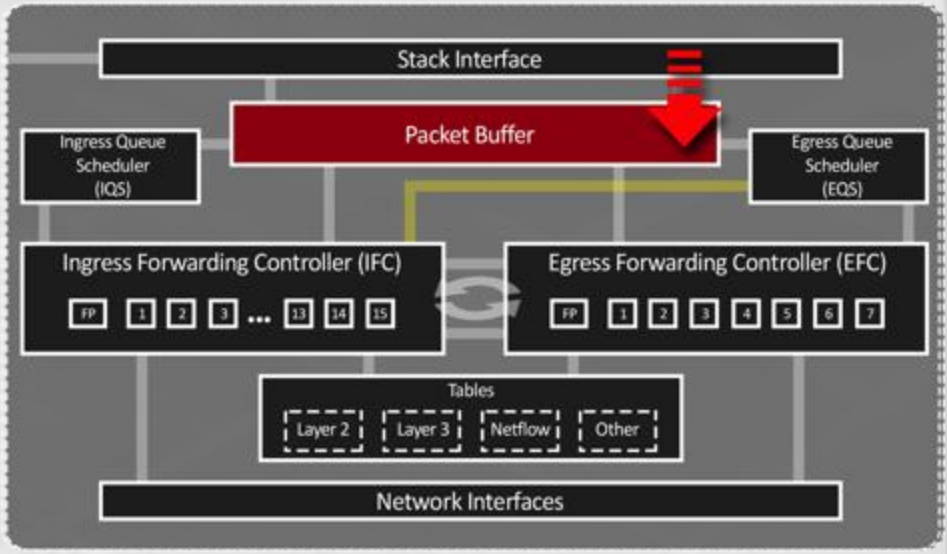


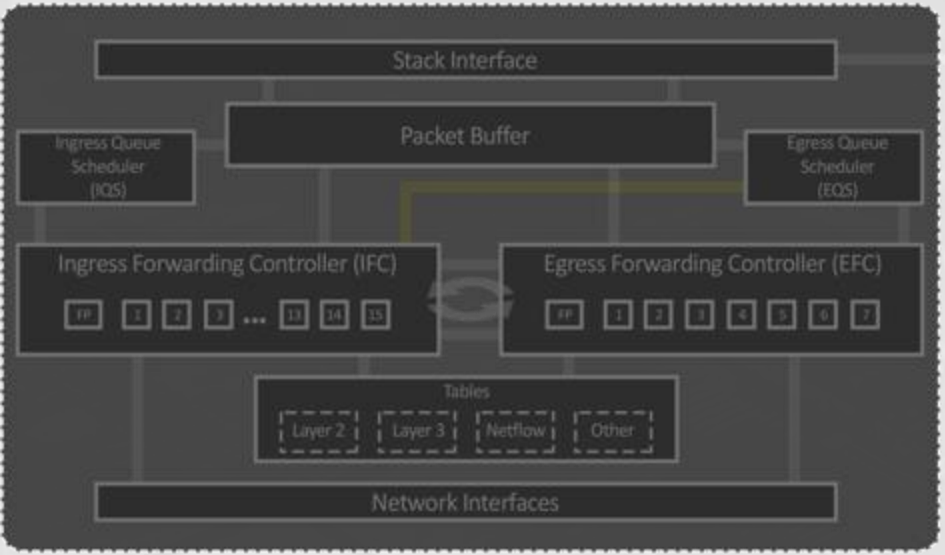


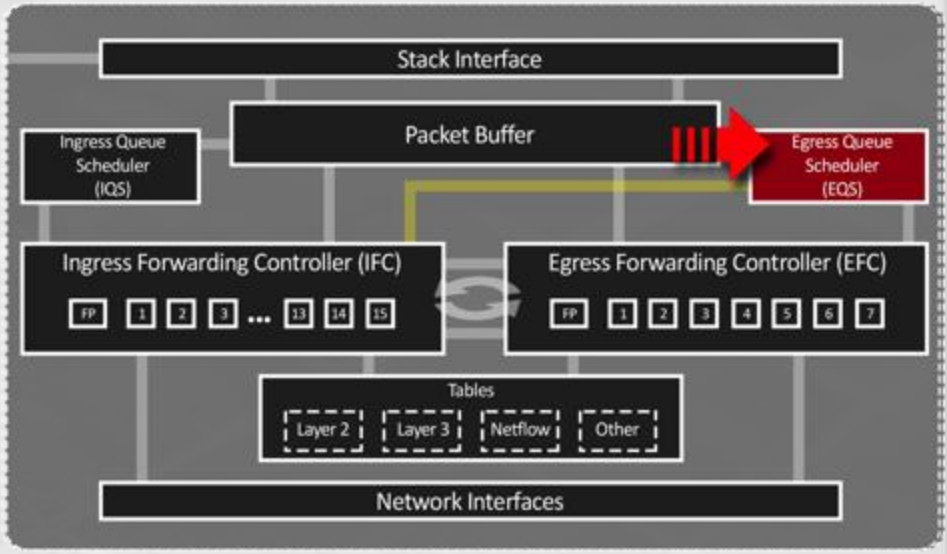



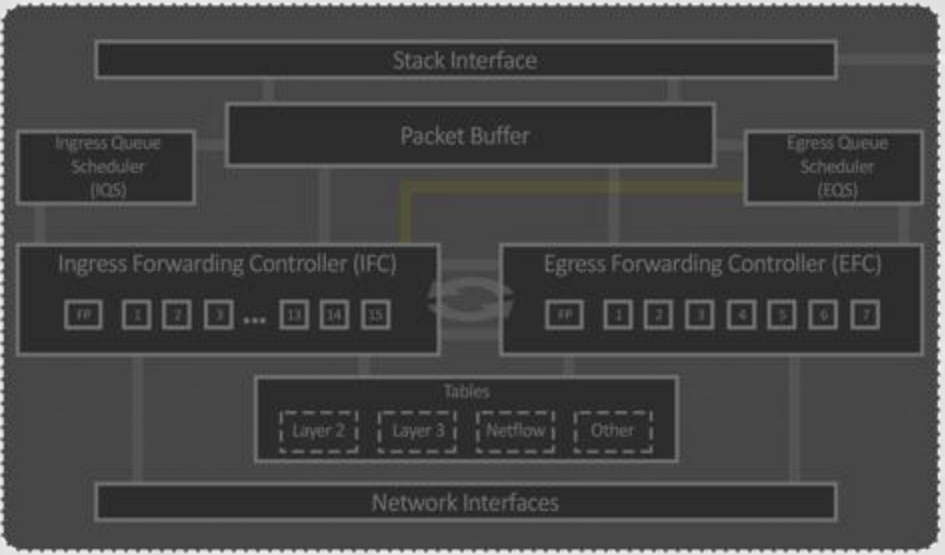



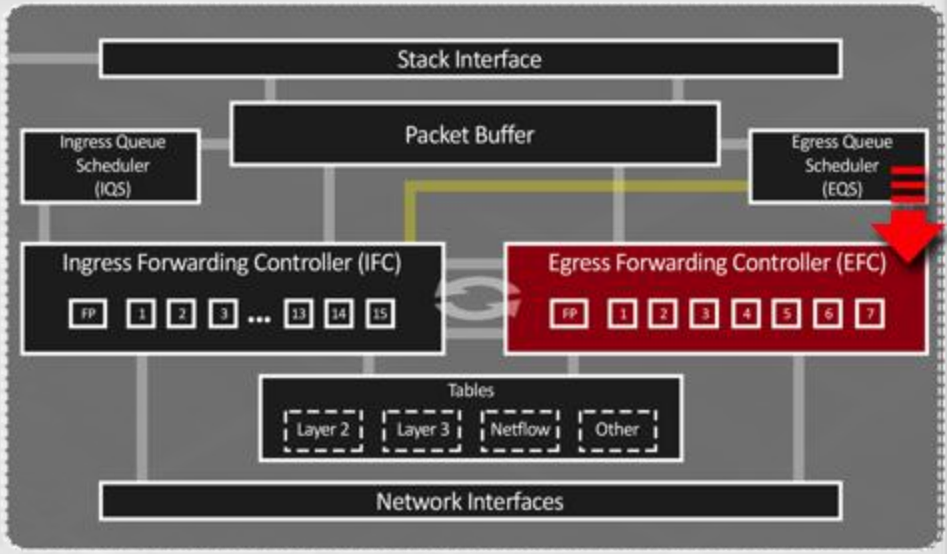



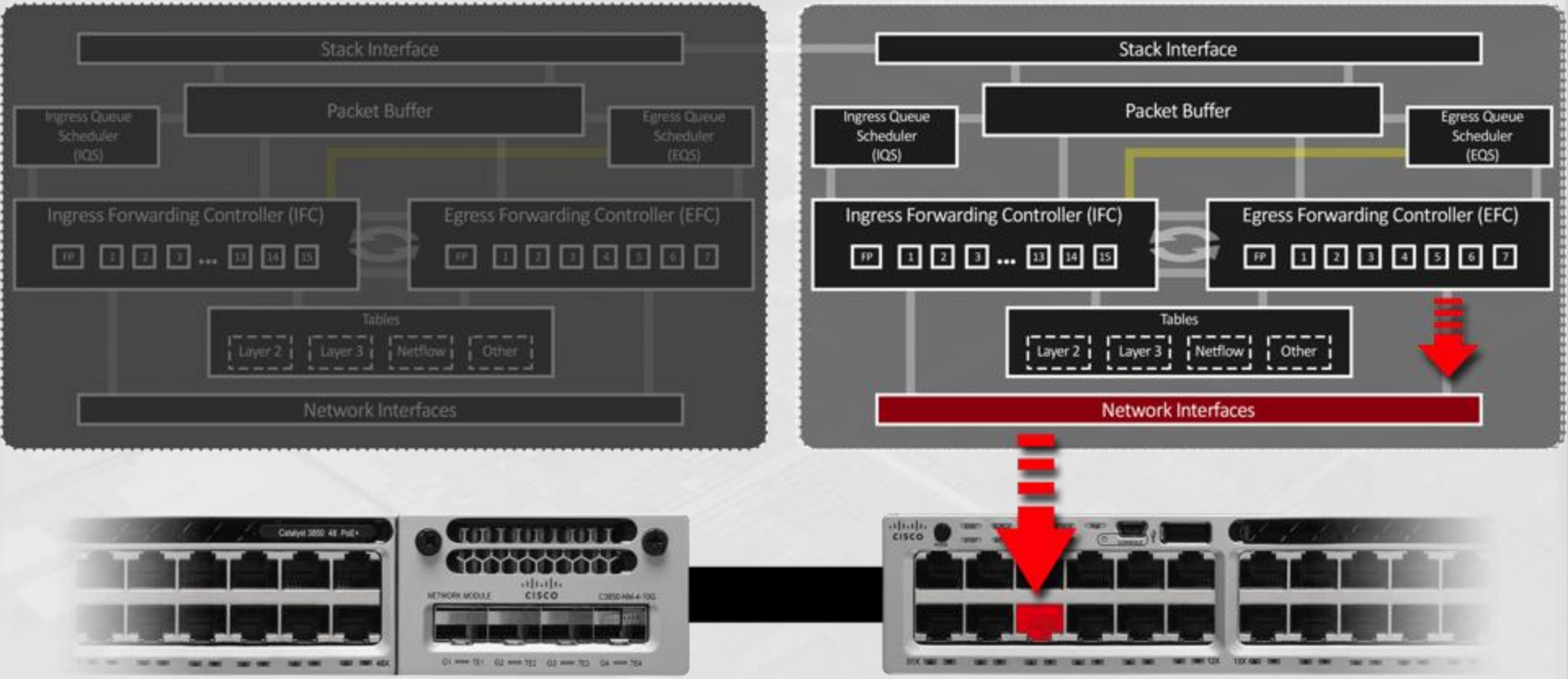



# What does this mean for me?

# UADP Programmable Hardware

# equals

# FLEXIBILITY

# INVESTMENT PROTECTION

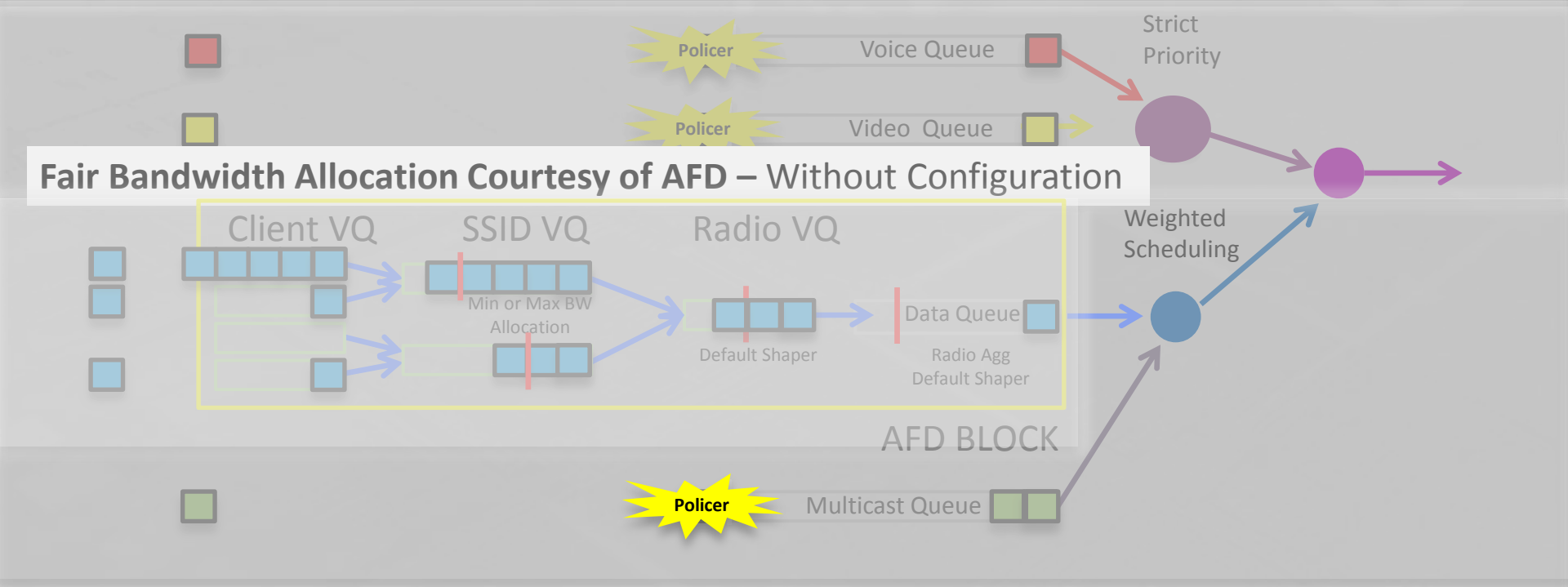
Approximate Fair Drop

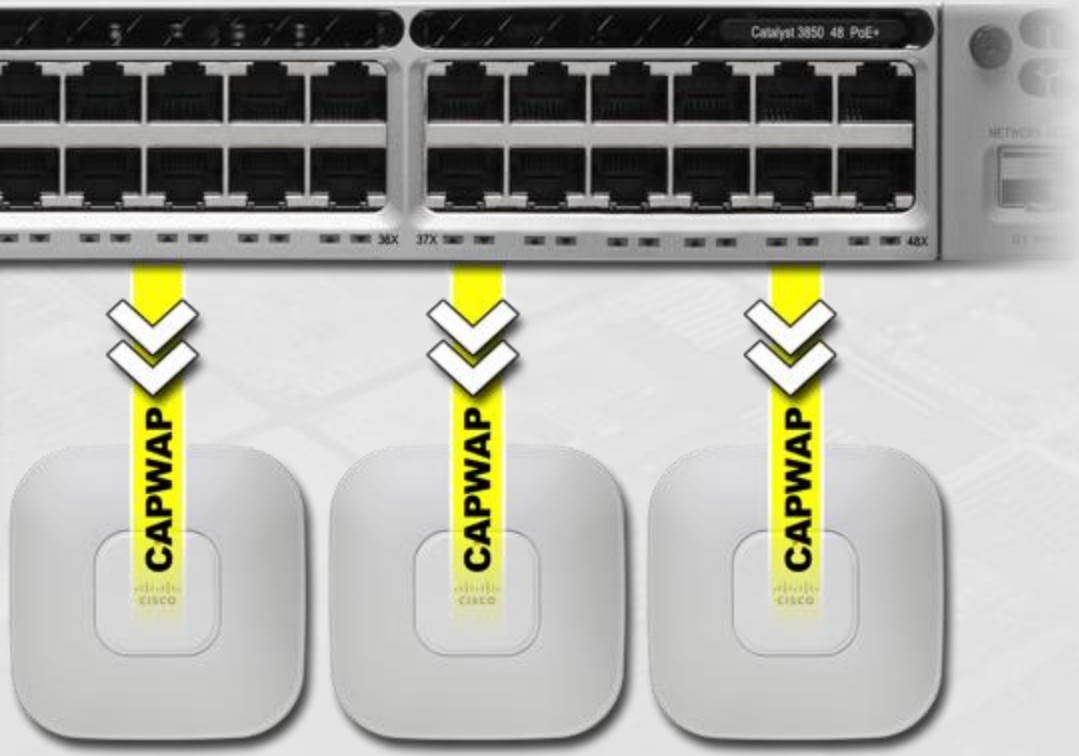
Fair Congestion Queue Bandwidth Sharing

Granular Per-User QoS

# UADP Advanced QoS

# UADP – Approximate Fair Drop



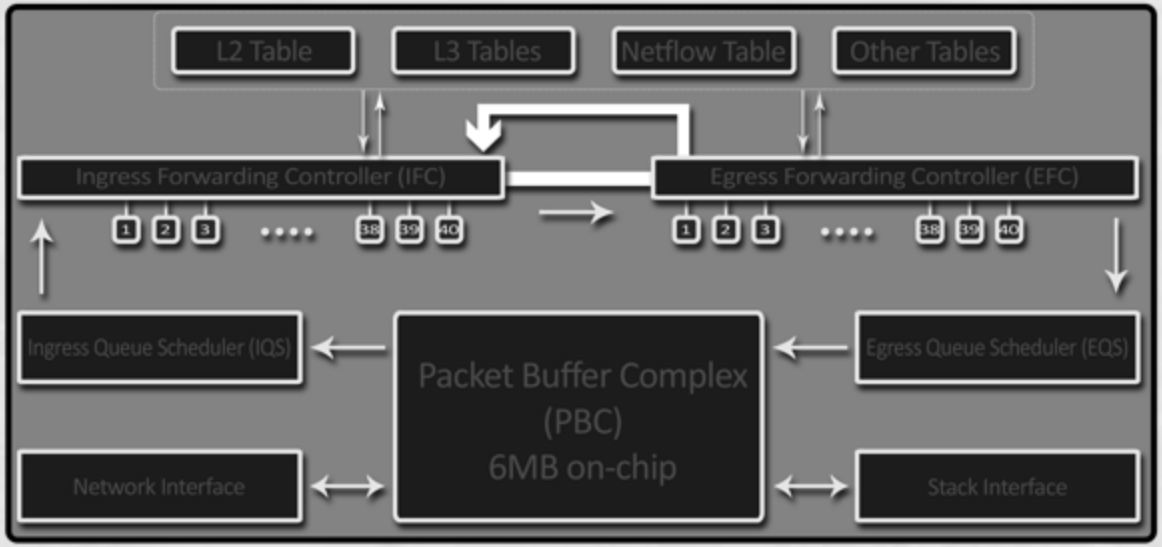



**Traffic Visibility**
e.g. Netflow

**Control**
Wired / Wireless QoS / Security

**Scalability**
802.11ac

# UADP Use Case




**VxLAN***
**TRILL***
**SPB***
**LISP***
**and more…**

* Not Committed


# Possible Future UADP Use Cases

WLAN Controller


Catalyst 3650

Catalyst 3850


Catalyst 4500

More to come


# UADP ASIC

## Where is it used?

# Why UADP?


Features and Flexibility

Performance

Scalability

# Where Else is Cisco Innovating in Silicon?

## A Few More Enterprise Examples ...

Monticello

Nexus 3548

Low Latency

Big Sur

Nexus 6000

High Density

10G/40G

F3 - Nexus 7000/7700

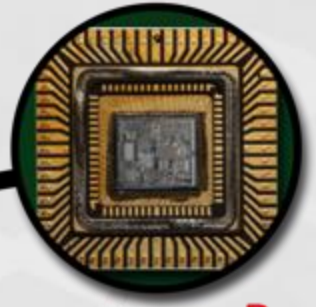
DC, 40G/100G

Psylocke

Cisco 7000

IP Phones

3rd Party XML Apps



Raven

Cisco 8K/9K

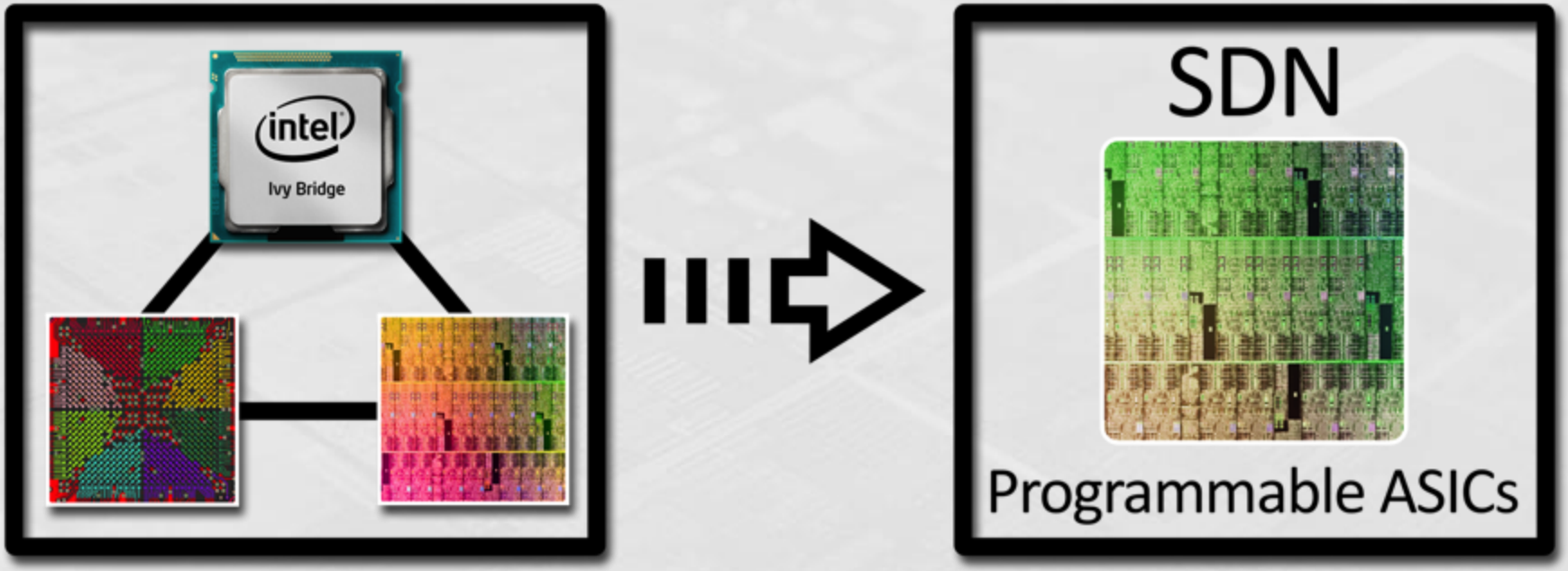
IP Phones

Std Video

Security

# AGENDA

Why ASICs?
How is an ASIC developed?
Merchant vs. Custom
Cisco ASIC History
The Move to Programmability
QFP
UADP
Summary




# Trend towards Programmability


VS.


Time to Market

Specific Customer Requirements

Innovation
Optimisation
Economies of Scale
Lead Market
Deliver Value


# Where ASICs Play…

Network Application Layer

Control Layer

Network Element Layer

# QFP


# UADP


# In-House Developed Programmable Silicon


# Critical Role of ASICs

# Q & A

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